Colour television

14GR1021/02B/02W/05B/05L/05W /07B/08B/10B/10L/10W /16B/16W/22B/22W

14GR1221/02B/05B/05L/05W/07B /08B/08L/08W/10B/10L/10W /16B/16L/16W/22B/22L/22W

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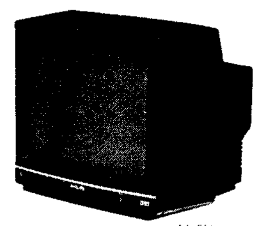
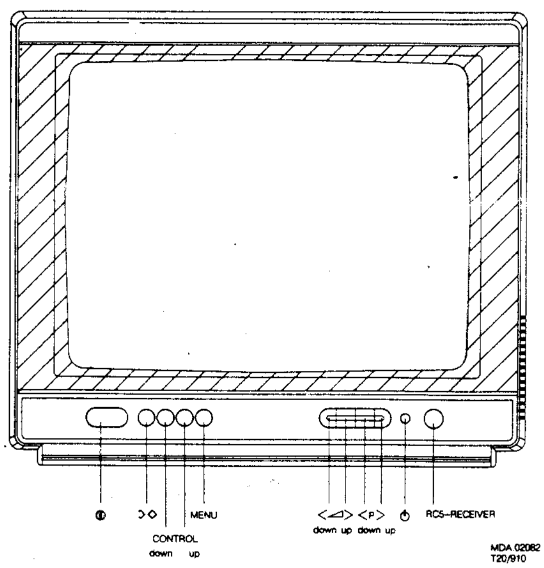


Service Manual 4822 727 16623 is herewith cancelled

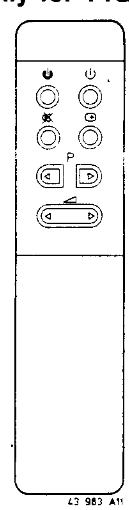
Service Manual

CHASSIS GR1-AX

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.



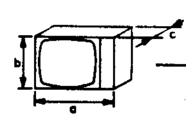
Only for 14GR1221



RC5701

→ VARIOUS

→ /02/08/10 PAL B/G
/05/07 PAL I
/22 PAL SECAM B/G



→ axbxc
354x314x362 mm

Documentation Technique Service Dokumentation Documentazione di Servizio Huolte-Ohje Manual de Servicio Manual de Servicio

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4822 727 16776
Printed in The Netherlands

PHILIPS

Published by Service Consumer Electronics

ITEM	VERSION /22	VERSION /03,/04, /06,/09, /11,/13	VERSION /02	VERSION /07	VERSION /16
1000	UV617	UV617	UV617	UV617	UV711
1020	x	–	–	–	–
1030	OFWG1961	OFWG1961	OFWG1961	OFWG1951	OFWG1961
1036	5.5MHz	5.5MHz	5.5MHz	6.0MHz	5.5MHz
1037	–	–	–	–	–
1038	5.5MHz	5.5MHz	5.5MHz	6.0MHz	5.5MHz
2002	1µ	1µ	1µ	1µ	1µ
2003	1µ	1µ	1µ	1µ	1µ
2006	6p8	–	6p8	–	–
2505	22µ	22µ	22µ	22µ	22µ
2515	22µ	22µ	22µ	22µ	22µ
2606	68µ	68µ	68µ	68µ	68µ
2782	–	–	–	–	–
3023	470K	470K	470K	470K	470K
3037	750R	750R	750R	750R	750R
3315	2R2	9R1	9R1	9R1	9R1
3503	2K4	2K4	2K4	2K4	2K4
3504	2K4	2K4	2K4	2K4	2K4
3506	43K	43K	43K	43K	43K
3511	3R6	3R6	3R6	3R6	3R6
3512	3R6	3R6	3R6	3R6	3R6
3668	9K1	9K1	9K1	9K1	9K1
3669	9K1	9K1	9K1	9K1	9K1
3781	–	–	–	–	–
3788	1M5	1M5	1M5	1M5	1M5
5035	–	–	–	–	–
5301	100µH	–	–	–	–
6638	BZX79–F36	BZX79–F36	BZX79–F36	BZX79–F36	BZX79–F36
6639	BZX79–F36	BZX79–F36	BZX79–F36	BZX79–F36	BZX79–F36
6640	BZX79–F33	BZX79–F33	BZX79–F33	BZX79–F33	BZX79–F33
6645	–	–	–	–	–
6646	–	–	–	–	–
6647	–	–	–	–	–
7528	BUT11AF	BUT11AF	BUT11AF	BUT11AF	BUT11AF
7610	BUK444–500B	BUK444–500B	BUK444–500B	BUK444–500B	BUK444–500B
7614	BF487	BF487	BF487	BF487	BF487
9003	–	X	X	X	X
9004	–	X	X	X	X

"X" = present
"–" = not present"

Continued on next page

ITEM	VERSION /05 SETS WITH "SV.." SERIAL NO	VERSION 08/10 SETS WITH "SV.." SERIAL NO	VERSION 08/10 SETS WITH "PM.." OR "ZB.." SERIAL NO	VERSION /05 SETS WITH "PM.." OR "ZB.." SERIAL NO
1000	U743	UV617	UV617	U743
1020	–	–	–	–
1030	OFWJ1953	OFWG1961	OFWG1961	OFWG1951
1036	6.0MHz	5.5MHZ	5.5MHz	6.0MHz
1037	–	–	–	
1038	6.0MHz	5.5MHZ	5.5MHz	6.0MHz
1524	–	–	T125MA	T125MA
2002	–	1µ	1µ	–
2003	–	1µ	1µ	–
2005	180n	180n	270n	270n
2006	–	–	–	–
2028	120p	120p	–	–
2044	10µ	10µ	4µ7	4µ7
2048	2n7	2n7	3n0	3n0
2110	470n	470n	–	–
2310	–	–	100n	100n
2322	1µ	1µ	220n	220n
2324	22µ	22µ	10µ	10µ
2341	22n	22n	–	–
2342	–	–	22n	22n
2390	120p	120p	100p	100p
2391	120p	120p	100p	100p
2392	120p	120p	100p	100p
2445	4n7	4n7	68n	68n
2505	33µ	33µ	22µ	22µ
2514	1nO	1nO	2n2	2n2
2515	100µ	100µ	22µ	22µ
2517	220µ	220µ	470µ	470µ
2527	680p	680p	1n	1n
2540	470µ	470µ	220µ	220µ
2606	68µ	68µ	68µ	68µ
2720	1n0	1n0	–	–
2734	–	–	1n0	1n0
2782	1µ	1µ	–	–
3023	390K	390K	470K	470K
3025	1K1	1K1	3K3	3K3
3034	1K3	1K3	–	–
3037	2K2	2K2	750R	750R
3052	1K8	1K8	1K0	1K8
3059	1K0	1K0	1K2	1K2
3061	2K2	2K2	–	–
3100	1R5	1R5	2R2	2R2
3303	–	–	2K2	2K2
3311	2K2	2K2	1K0	1K0
3315	9R1	9R1	9R1	9R1
3322	430K	430K	–	–
3323	–	–	680K	680K
3390	100R	100R	–	–
3391	100R	100R	–	–
3392	100R	100R	–	–
3393	270R	270R	–	–
3503	4K3	4K3	2K4	2K4
3504	2K0	2K0	2K4	2K4
3506	13K	13K	43K	43K
3511	2R4	2R4	3R6	3R6
3512	2R7	2R7	3R6	3R6
3513	2K2	2K2	–	–
3520	33R	33R	47R	47R
3521	4K7	4K7	–	–

ITEM	VERSION /05 SETS WITH "SV.." SERIAL NO	VERSION 08/10 SETS WITH "SV.." SERIAL NO	VERSION 08/10 SETS WITH "PM.." OR "ZB.." SERIAL NO	VERSION /05 SETS WITH "PM.." OR "ZB.." SERIAL NO
3531	51R	51R	–	–
3532	51R	51R	100R	100R
3535	8R2	8R2	2R7	2R7
3646	150R	150R	–	–
3668	9K1	9K1	9K1	9K1
3669	9K1	9K1	9K1	9K1
3670	1K6	1K6	1K0	1K0
3671	1K0	1K0	–	–
3675	–	–	22K	22K
3716	1K6	1K6	620R	1K6
3718	27K	27K	33K	27K
3725	27K	27K	22K	27K
3726	30K	30K	39K	39K
3730	240K	240K	470K	470K
3752	–	1K2	1K2	–
3753	–	1K2	1K2	–
3754	–	2K7	2K7	–
3760	2K7	2K7	3K9	3K9
3762	560R	560R	680R	680R
3778	1K	1K	–	–
3781	150K	150K	–	–
3788	3M	3M	1M5	1M5
3790	–	–	10K	10K
3791	39R	39R	–	–
3799	–	–	1K	1K
5035	–	–	–	–
5038	10µ	10µ	4µ7	4µ7
5301	–	–	–	–
5519	33µ	33µ	3µ9	3µ9
5544	–	–	10µ	10µ
5621	0µ7	0µ7	1µ	1µ
5752	–	10µ	10µ	–
5753	–	10µ	10µ	–
6521	BAT85	BAT85	–	–
6545	BZX79–F5V1	BZX79–F5V1	–	–
6602	BY627	BY627	1N4005GP	1N4005GP
6603	BY627	BY627	1N4005GP	1N4005GP
6604	BY627	BY627	1N4005GP	1N4005GP
6605	BY627	BY627	1N4005GP	1N4005GP
6638	BZX79–B36	BZX79–B36	BZX79–F36	BZX79–F36
6639	BZX79–B36	BZX79–B36	BZX79–F36	BZX79–F36
6640	BZX79–B30	BZX79–B30	BZX79–F33	BZX79–F33
6645	–	–	–	–
6646	–	–	–	–
6647	–	–	–	–
6671	BZX79–B5V6	BZX79–B5V6	BZX79–F4V3	BZX79–F4V3
6675	BZX79–F5V1	BZX79–F5V1	–	–
6736	1N4148	–	–	1N4148
7100	BC558	BC558	–	–
7528	2SC3795B	2SC3795B	BUT11AF	BUT11AF
7610	BUK444–500B	BUK444–500B	BUK444–500B	BUK444–500B
7614	BF487	BF487	BF487	BF487
7674	BC548	BC548	–	–
7750	–	LA7910	LA7910	–
7785	X2402	X2402	ST24C02CP	ST24C02CP
9003	X	X	X	X
9004	X	X	X	X

"X" = present
"–" = not present"

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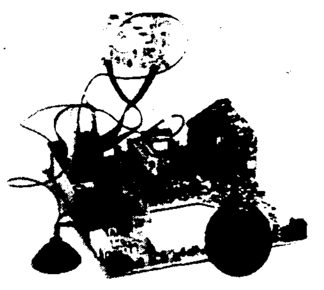

Circuit Description

CONTENTS

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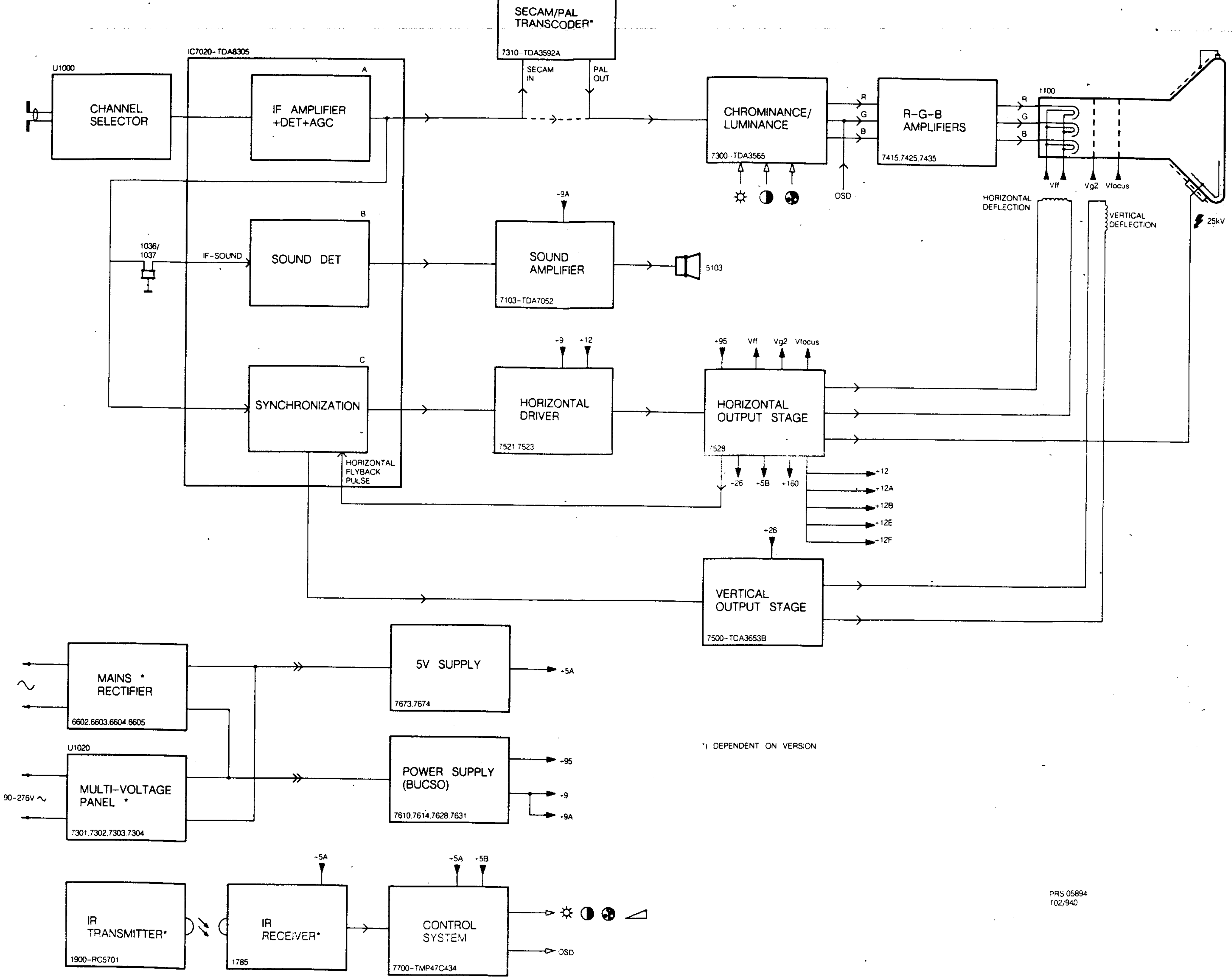
CS 26 069 GB

1. BLOCK DIAGRAM

All the circuits of the GR1AX chassis are contained on a monochassis, with the exception of the cathode-ray tube PCB, the SECAM/PAL transcoder and the multivoltage PCB U1020.
The SECAM/PAL transcoder is only present in equipment suitable for receiving SECAM signals and the multivoltage PCB is only present if the equipment is suitable for mains voltages of 90–276V.
The monochassis contains the following blocks:

1. There is a channel selector in position 1000.
2. There is an IC of type TDA8305 in position 7020. This IC contains the MF amplifier and detector, the MF sound detector and the synchronisation circuit.
3. The chrominance/luminance processor is in position 7300.
4. The RGB amplifiers are contained on the cathode-ray tube PCB. The cathode-ray tube PCB is suitable for various types of 14" cathode-ray tubes:
    1. A34JRH61X(Y)
    2. A34EAC01X45
    3. 370KSB22-SYB

   For 20"/21" the cathode-ray tube PCB is modified because this is not pin compatible.
5. The sound amplifier which supplies an output power of 1W is in position 7103.
6. The horizontal output stage TS7528 is controlled by the horizontal control stage TS7521/TS7523. The horizontal output stage supplies:
    1. the horizontal deflection current
    2. the high voltage
    3. the focus voltage
    4. various derived supply voltages
7. The vertical output stage IC7500 supplies the vertical deflection current.
8. The power supply which is not mains isolated of the BUCSO type (BUck Converter Self Oscillating) supplies the main supply +95 and several derived voltages.
   A separate 5V supply circuit supplies the 5-volt standby power.
9. The operating system (VST) is based on the microcomputer IC7700.


SECAM/PAL TRANSCODER*
7310-TDA3592A
SECAM IN
PAL OUT
IC7020-TDA8305
U1000
CHANNEL SELECTOR
A
IF AMPLIFIER +DET+AGC
CHROMINANCE/ LUMINANCE
7300-TDA3565
R
G
B
R-G-B AMPLIFIERS
7415.7425.7435
1100
Vff
Vg2
Vfocus
OSD
HORIZONTAL DEFLECTION
VERTICAL DEFLECTION
25kV
+9A
B
1036/ 1037
IF-SOUND
SOUND DET
SOUND AMPLIFIER
7103-TDA7052
5103
+9
+12
+95
C
SYNCHRONIZATION
HORIZONTAL DRIVER
7521.7523
HORIZONTAL OUTPUT STAGE
7528
HORIZONTAL FLYBACK PULSE
+26
+5B
+160
+12
+12A
+12B
+12E
+12F
VERTICAL OUTPUT STAGE
7500-TDA3653B
MAINS * RECTIFIER
6602.6603.6604.6605
5V SUPPLY
7673.7674
+5A
U1020
MULTI-VOLTAGE PANEL *
7301.7302.7303.7304
90-276V ~
POWER SUPPLY (BUCSO)
7610.7614.7628.7631
-95
-9
+9A
*) DEPENDENT ON VERSION
IR TRANSMITTER*
1900-RC5701
IR RECEIVER*
1785
CONTROL SYSTEM
7700-TMP47C434
+5A
+5B
OSD
PRS 05894
102/940

2 POWER SUPPLY

2.1 Mains rectifying device and degaussing

The mains voltage is supplied via mains switch SK1, fuse VL1600 and interference filter C2600–L5601 to the full-wave rectifier circuit D6602 to D6605 (see appendix 1). The capacitors C2603 and C2605 are for limiting peak voltage.
The rectified voltage which is produced over smoothing capacitor C2606 is supplied to the main power circuit and the 5V circuit.
The mains voltage is also supplied to the degaussing circuit R3602, L5600. When it is switched on, R3602 is cold. The current which flows through the degaussing coil L5600 is initially very high (approx. 5A), but very quickly decreases to several milliamperes as a result of the quick heating up of the PTC, R3602b. R3602a is thermally coupled with R3602b and ensures that the PTC stays warm.

2.2 Main power supply

The power supply used in GR1–AX is of the BUCSO (=**BU**ck **C**onverter **S**elf **O**scillating) type. It is a self–oscillating power supply, however it is not mains isolated. The following mains voltages are available:

–220–240V (direct)
–90–140 and 160–276V (with a transformer, see section 2.3)

The power supply is 97.5V (+95) for the line output stage and 10V(+9) for the sound amplifier. In addition, the supply is protected against output voltages which are too high and against short circuits.
The output voltage is 97.5V in the unloaded state. In standby the main supply is completely switched off and the microcomputer is powered by 5V.

2.2.1 Basic operation (fig 2.1)

If the FET 7610 conducts, current I_1 will start to flow, which means that C_2660 is charged. Magnetic energy is now also built up in the transformer 5610.At a given moment the FET will block and then T5610 will supply power to C2660 via D6620 (see fig. 2.2).
C2660 is thus supplied with current when the FET is conducting and blocking. The current variation is shown in fig. 2.2.
Time t_2 is $\approx 2t_1$, as during t_1 the voltage over the coil is approximately 200V (=300–95V) and during $t_2 \approx 100V$ (UC2660).

2.2.2 Start of the oscillator

A U_{GS} voltage must first be generated so that the FET can start conducting. This is done using a voltage divider R3610, R3613,
R3611 and D6613 (see fig. 2.3). In order to explain the formation of the starting voltage, use is made of the equivalent–circuit diagram shown in fig. 2.4. The voltage is first stabilised to U_1 (=15V) using D6613 and is then divided over the two resistors R3613/R3611. The U_{GS} voltage is thus (56/176)*15=4.77V. This is sufficient to start the FET conducting. Point 2 of T5610 is now positive as compared with point 12.

Once the FET is conducting, this is made to continue conducting as follows (see fig. 2.5)

If the unit is working normally, there is 97.5V on pin 12 of T5610. There is 300V on pin 2 and a voltage of 30V will be produced by the winding ratio over winding 13–2. As a result of this, current I charges the capacitor 2613. As a result of this current, the U_{gs} voltage increases, which means that the FET continues to conduct. The U_{GS} voltage is limited by a zener diode of 10V (D6610).

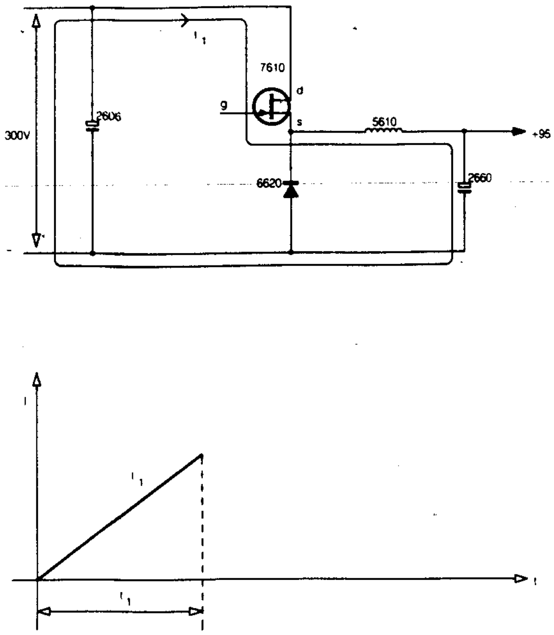


Fig. 2-1

PRS 06258
T02/941

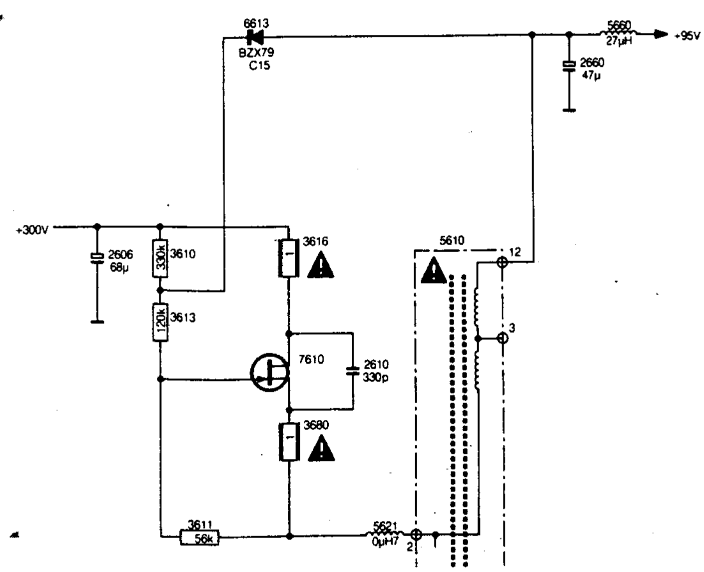


Fig. 2-3

ESV 00195
T02/941

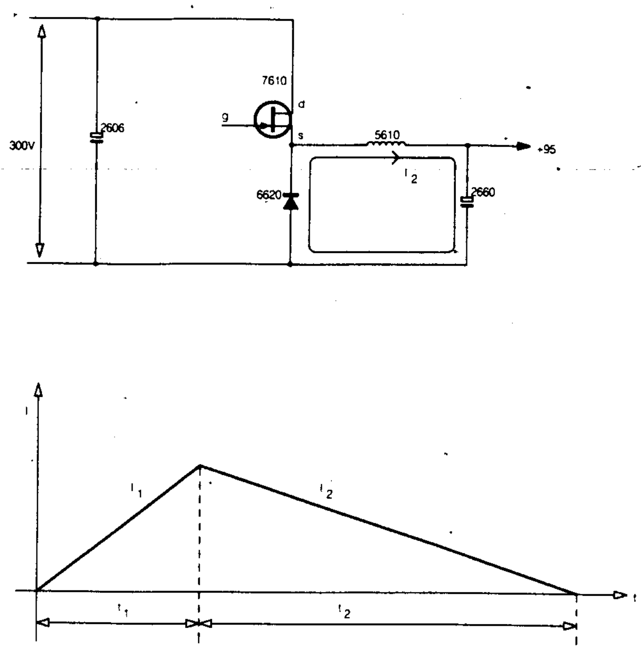


Fig. 2-2

PRS 06257
T02/940

+95V

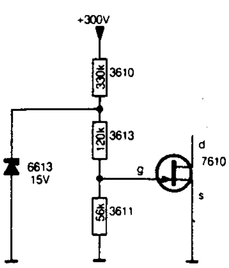


Fig. 2-4

00195
941

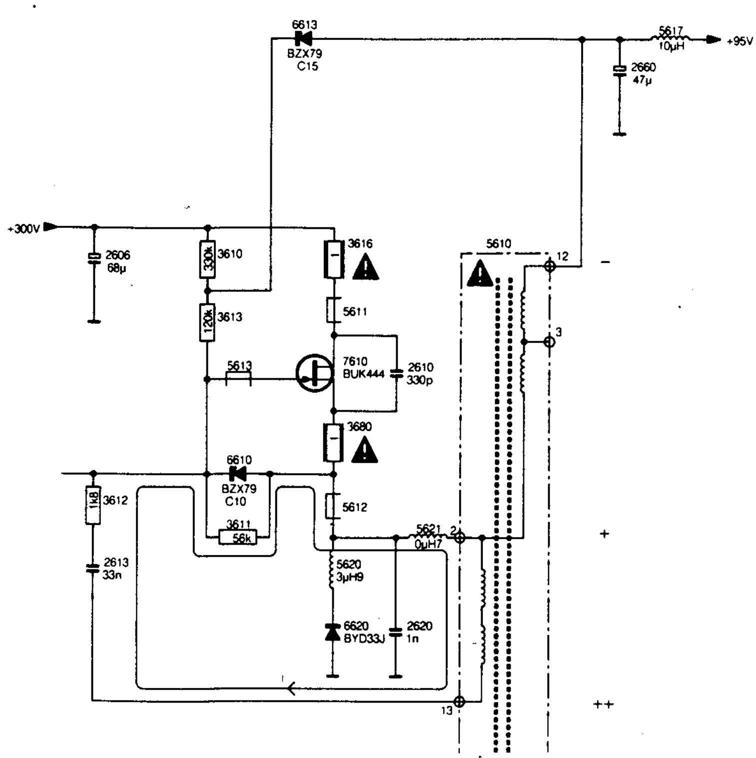


Fig. 2-5

ESV 00193
T02/942

2.2.3 Pulse–width modulation circuit

Once the FET 7610 is conducting, this must also be switched off again. This is done in the following way..

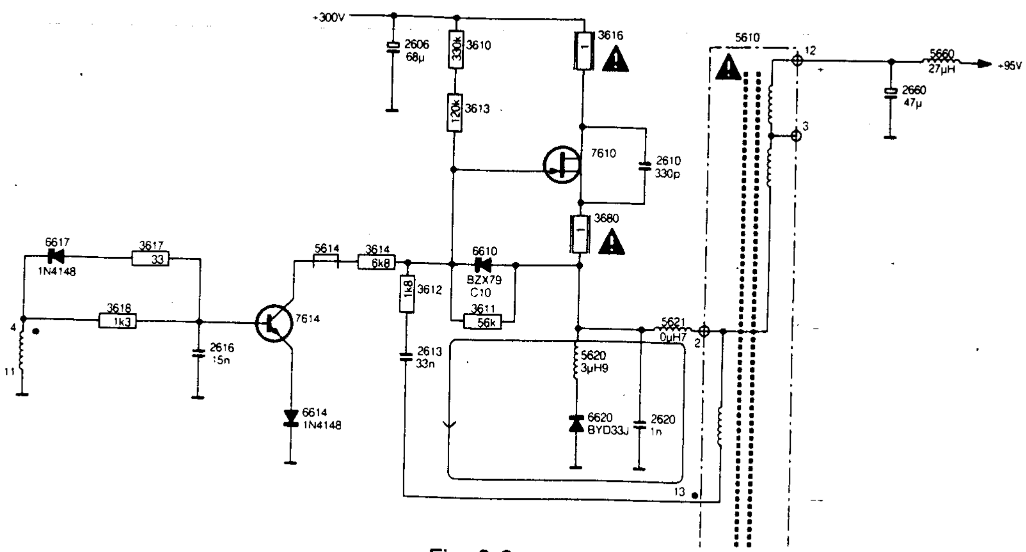


Fig. 2-6

ESV 00194
T02/942

Because of the magnetic coupling, when TS7610 is conducting current will also flow through winding 4–11. This current charges via 3618 C2616. If the voltage is 1.2V over C2616, TS7614 starts to conduct so that the U_{GS} voltage becomes low and TS7610 will block. 1.2V is needed to make TS7614 conductive, because of the threshold voltages of D6614+TS7614.
If TS7610 blocks, then the energy built up in T5610 is supplied to the load via D6620.
If TS7610 is switched off, then there is a positive voltage on pin 12 as compared with pin 2. Because of the winding direction there will also be a negative voltage over winding 13–2. This voltage charges C2613 and, as a result of this discharge current, a negative voltage is produced over R3611, which again is limited by D6610 at $-\approx 0.6$V. Because U2–12 is now negative, U4–11 will also become negative. In this way C2616 can be discharged once more via D6617/R3617.
Here it must be noted that when starting up the load should not be too great (thus take care when carrying out repair), as then the voltage is $\approx$300V over winding 2–12. There is thus a considerable voltage over winding 4–11 of T5610 and TS7610 is switched off quickly each time. The output voltage will now not be higher than $\approx$5V. The output voltage must be more than 15V if the circuit is to take over with C2613/R3612. The energy will then be transferred to the load.

The circuit in fig. 2.7a will then start to oscillate. The voltage on pin 2 of T5610 varies, as shown in fig. 2.7b. At time t^1 C2620 is charged to 97.5V via T5610 by the charge of C2660. During this charging process, energy is also built up in T5610. T5610 will also let this energy flow off to C2620, so that the voltage over C2620 increases further. At t^2 the voltage at pin 2 is positive as compared with pin 12 and because of the winding ratio pin 13 will also be positive as compared with pin 2.
At time t^3 the voltage U^{13-2} is again 20V, which once more switches on the FET. This means that U^A becomes 300V and the whole process can start again from the beginning.

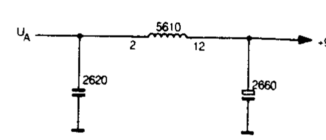


Fig. 2-7a

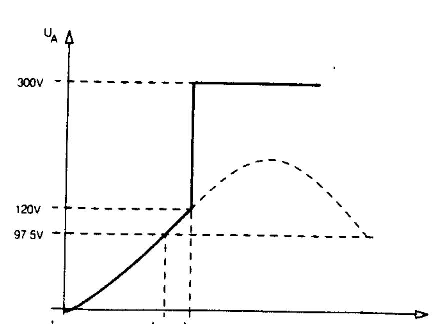


Fig. 2-7b

PRS 06259
T02/940

2.2.4 Control of the output voltage

The output voltage can be set using R3625. This is used to determine the voltage level at which TS7628 must become conductive.
When operating normally TS7628 will start conducting when the output voltage exceeds 97.5 V. A current will then flow to the base of TS7614 so that this starts to conduct and TS7610 is switched off.

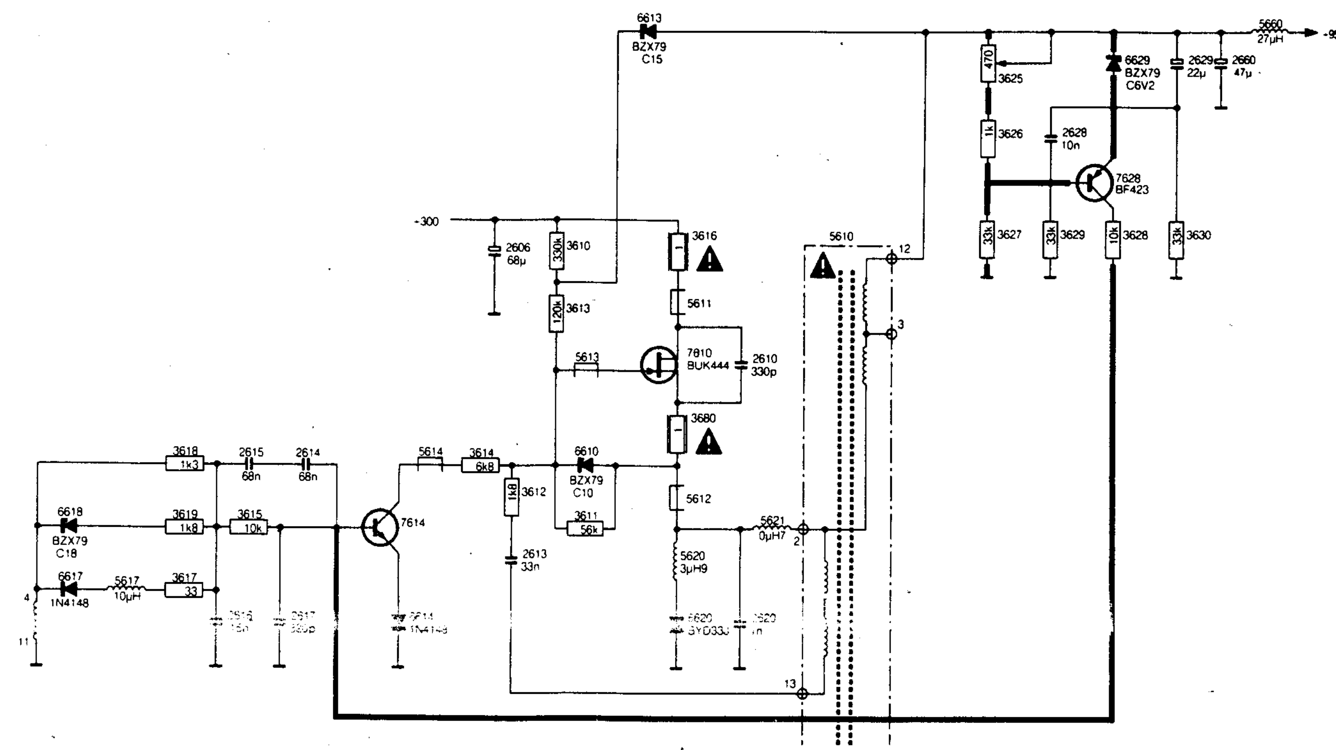


Fig. 2-8

ESV 00192
T02/942

2.2.5 Overvoltage protection (see fig. 2.9)

The overvoltage protection circuit is based on thyristor 6641. The overvoltage protection can be controlled in 2 ways:

- if the filament voltage becomes too high because of some fault or other, then diodes D6646 and D6647 become conductive so that TH6641 starts conducting.
- If 97.5V becomes too high, then thyristor 6641 is made conductive via D6638, D6639 and D6640.

In the GR1AX units only one of these two methods is used. The power supply is now almost short circuited. Approximately 1.5V remains as the output voltage. If the protection is active, then the BUCSO operates in short–circuit mode (see 2.2.9).
However, the remaining voltage is not sufficient to maintain TH6641 conductive. The thyristor stops conducting. The power supply is then started again and the protection becomes active and the supply will again be short circuited. As a result of this a hiccup effect will be produced. In order to prevent this hiccup effect, TH6641 is maintained conductive using D6643 and D6644. These two diodes ensure that the thyristor obtains sufficient current. As a result of this the 5 V will also drop.
D6642 must prevent current flowing to the load via this path.

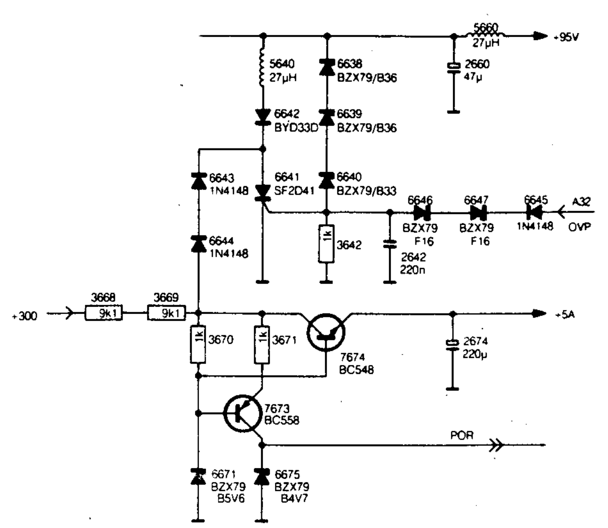


Fig. 2-9

ESV 00190
T02/941

2.2.6. 5-volt power supply (see fig. 2.9)

The supply voltage for the microcomputer is derived directly from the rectified mains voltage.
D6671 serves as a reference of 5.6V for the series stabilisation transistor 7674 for the +5A (+5V).

2.2.7. P.O.R. (fig. 2.10)

In order to make sure that the microcomputer starts from an initialised state after it has been switched on, a Power On Reset (P.O.R.) pulse should be supplied to pin 33. Once the supply voltage is present, pin 33 should remain low for 1 msec.
After switching on, the +5V power supply will appear but, because transistor 7673 blocks, pin 33 of the microcomputer will still be low.
Transistor 7673 remains blocked.
If the supply voltage reaches the zener point (5.6V) of zener diode 6671, transistor 7673 will become conductive. Limited by zener diode 6675, the P.O.R. signal now becomes high (4.7V).
While pin 33 is low, the oscillator of the microcomputer starts, because the supply voltage of the microcomputer is supplied via the conducting transistor 7674. The microcomputer starts to operate at a supply voltage of 4.5V.

2.2.8 Standby (see appendices 1 and 2)

The TV can be set to standby using the remote control. The µC IC7700 makes pin 19 low (and also pin 20 for the control of the LED 6757) and TS7631 starts conducting. TS7610 is completely switched off via TS7614
There is still voltage (≈5V) at the +95 because of R3610–D6613.

2.2.9 Short–circuit protection

If the +95 is short circuited, then the power supply is not interrupted. There is then suddenly a much greater voltage over winding 4–11 of T5610. TS7614 starts conducting, which means that the gate of 7610 is no longer controlled. TS7610 blocks and the power supply switches off.
Because C2613 must first be discharged and then recharged by a positive voltage, TS7610 can only start conducting again after ≈1 msec.

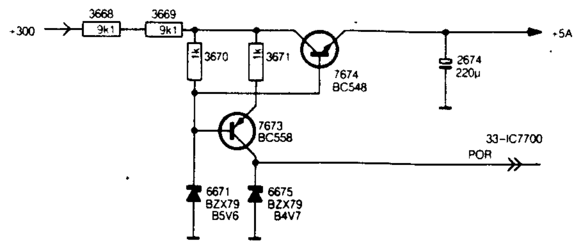


Fig. 2-10

ESV 00191
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2.3 110V converter

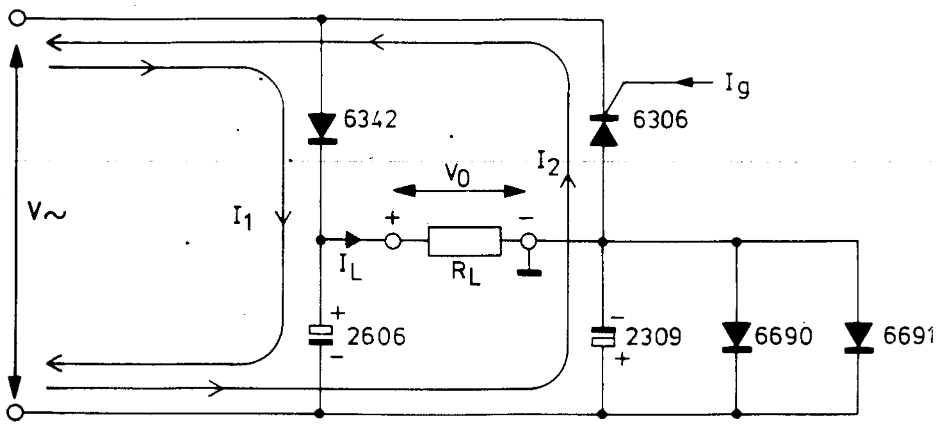


Fig. 2-11 45 037 C11

2.3.1 Basic function

The automatic voltage converter is based on a Greinacher voltage doubler. A simplified diagram is given in fig. 2.11. The circuit is controlled by a voltage detection circuit that ensures that from thyristor 6306 I_g=0 if the supplied voltage is between 160 and 276V and I_g>0 if the mains voltage is between 90 and 140V.

If I_g=0, then thyristor 6306 does not take part and the circuit operates as a single–phase rectifying device via D6342, C2606. The load current is removed via R_L and D6690/D6691. For safety reasons two diodes are positioned in parallel, as C2309 should not be negatively charged.

If the gate current I_g>0, thyristor 6306 will start conducting and the circuit will operate as a voltage doubler.

This works as follows:

During the positive half of the mains voltage, D6342 conducts and C2606 is charged positively (up to V_{max}) with the polarity as indicated in the figure. During the negative period of the mains voltage C2309 is charged by I_2 (up to V_{max}), see figure..

The output voltage V_o is now 2*V_{max} of the mains voltage with which the voltage was doubled.

The operation of the mains voltage detection circuit is explained using fig. 2.12.

The mains voltage is rectified via D6303/D6304 and C2301 is charged to 140V (for 110V mains voltage) or 290V (for 220V mains voltage). A voltage V_z of 6.8V is derived from this rectified voltage via R3301, R3302, D6344 and zener diode D6307 which is parallel to C2302. As soon as V_z is present, the thyristors 6305 and 6306 will be lit via R3311 and voltage doubler R3346 and R3345, so that the voltage doubling described above takes place.

Thyristor 6306 is controlled by thyristor 6305 because the gate current at low mains voltage is not sufficient to light thyristor 6306.

If the mains voltage is more than 150V, the voltage cannot be doubled and thyristor 6306 must be switched off.

This can be done by switching V_z off. V_z can be switched off in the following two ways:

1. If the rectified mains voltage rises above 190V (mains voltage >140V), the voltage on the cathode of the zener diode 6308 becomes more than 6.2V, so that this diode and thus also TS7303 start to conduct and V_z is switched off. TS7304 ensures that no current flows through the zener diode 6308 at a lower mains voltage.
2. If method 1 does not work because of a defect, the following should take place:

   At 140V mains voltage, after rectification via diodes 6303, 6304, a direct current will flow via R3301, R3302 through the measuring resistor 3344 and then via 3348, 3349 to the chassis earth 2V3.

   This current through 3344 is so great that the voltage for it is smaller than the zener voltage 6.2V of 6344 and the b–e voltage.

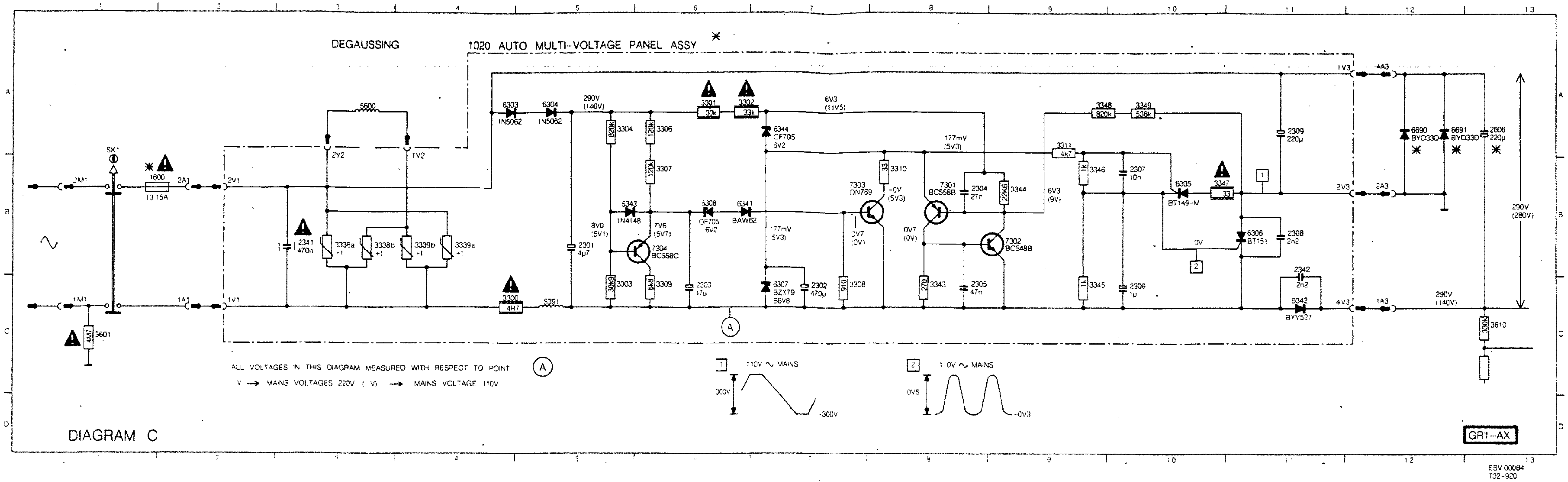
   TS7301 will not conduct and will thus leave V_z undisturbed. V_z will light thyristor 6305 and the voltage is doubled via TH6306.

   However, if the mains voltage is 220V, I will increase, which means that U^{3344} increases. D6344 will conduct, TS7301 will conduct and this will make TS7302 conduct. The underneath of R3344 is now resting on the virtual earth point A, which means that the current increases through R3344. As a result of this, U^{3344} will increase and TS7301 will conduct further via 6344. In this way the circuit becomes stable.

Note:

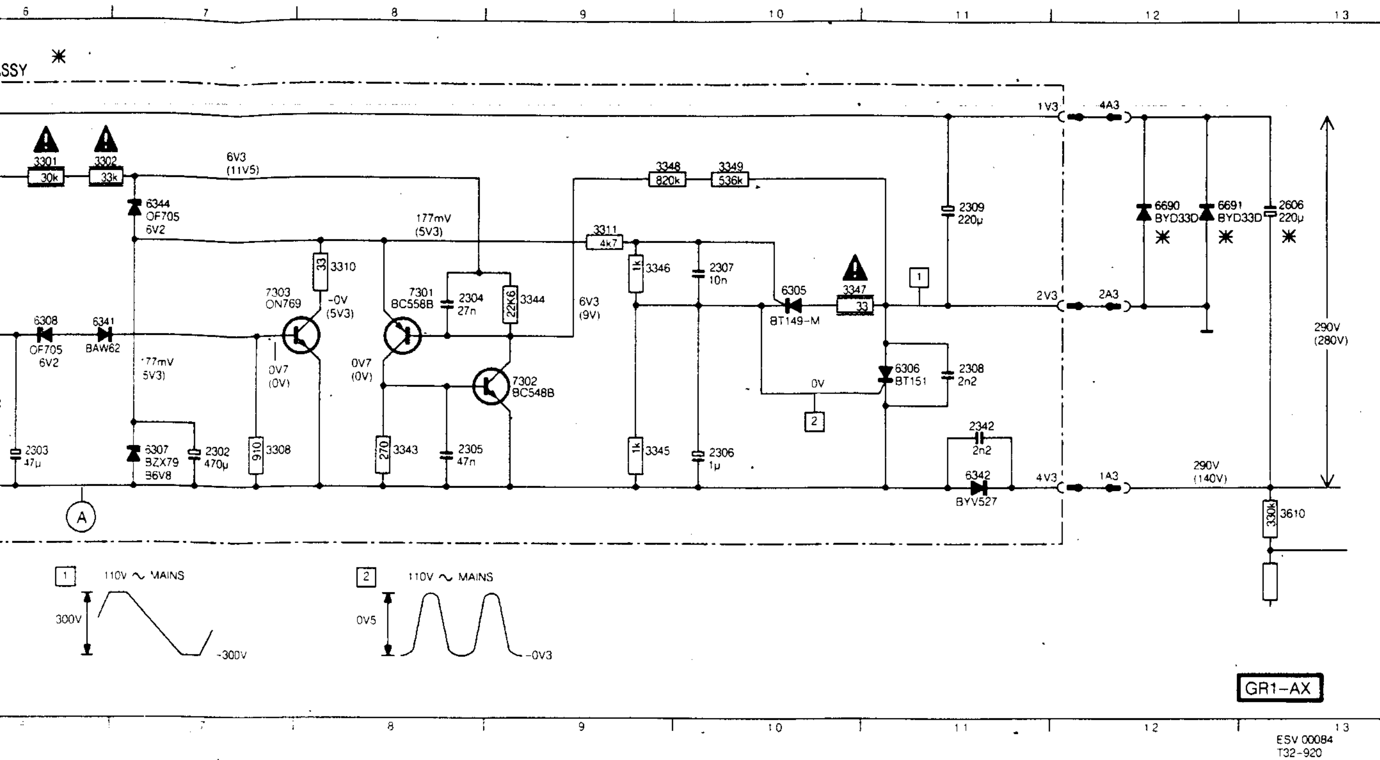
Because of the tolerance in components, it may happen that the voltage doubling does not work properly if the mains voltage is between 140 and 160V. This area falls outside the specification.

MULTI VOLTAGE PANEL



1600-B1	MX -A12
2301-B5	SK1 -B1
2302-C7	V2 -B3
2303-C6	V3 -A12
2304-B8	
2305-C8	
2306-C10	
2307-B10	
2308-B11	
2309-A11	
2341-B3	
2342-C11	
2606-A13	
3300-C4	
3301-A6	
3302-A6	
3303-C5	
3304-A5	
3306-A6	
3307-B6	
3308-C7	
3309-C6	
3310-B8	
3311-A9	
3338-B3	
3339-B4	
3343-C8	
3344-B9	
3345-C9	
3346-B9	
3347-B10	
3348-A9	
3349-A10	
3601-C1	
3610-C13	
5391-C5	
5600-A3	
6303-A5	
6304-A5	
6305-B10	
6306-B11	
6307-B7	
6308-B6	
6341-B7	
6342-C11	
6343-B6	
6344-A7	
6690-A12	
6691-A12	
7301-B8	
7302-B8	
7303-B7	
7304-B5	
M1 -B1	

Fig. 2-12



1600-B1
2301-B5
2302-C7
2303-C6
2304-B8
2305-C8
2306-C10
2307-B10
2308-B11
2309-A11
2341-B3
2342-C11
2606-A13
3300-C4
3301-A6
3302-A6
3303-C5
3304-A5
3306-A6
3307-B6
3308-C7
3309-C6
3310-B8
3311-A9
3338-B3
3339-B4
3343-C8
3344-B9
3345-C9
3346-B9
3347-B10
3348-A9
3349-A10
3601-C1
3610-C13
5391-C5
5600-A3
6303-A5
6304-A5
6305-B10
6306-B11
6307-B7
6308-B6
6341-B7
6342-C11
6343-B6
6344-A7
6690-A12
6691-A12
7301-B8
7302-B8
7303-B7
7304-B5
M1 -B1

MX -A12
SK1 -B1
V2 -B3
V3 -A12

Fig. 2-12

MULTI VOLTAGE PANEL

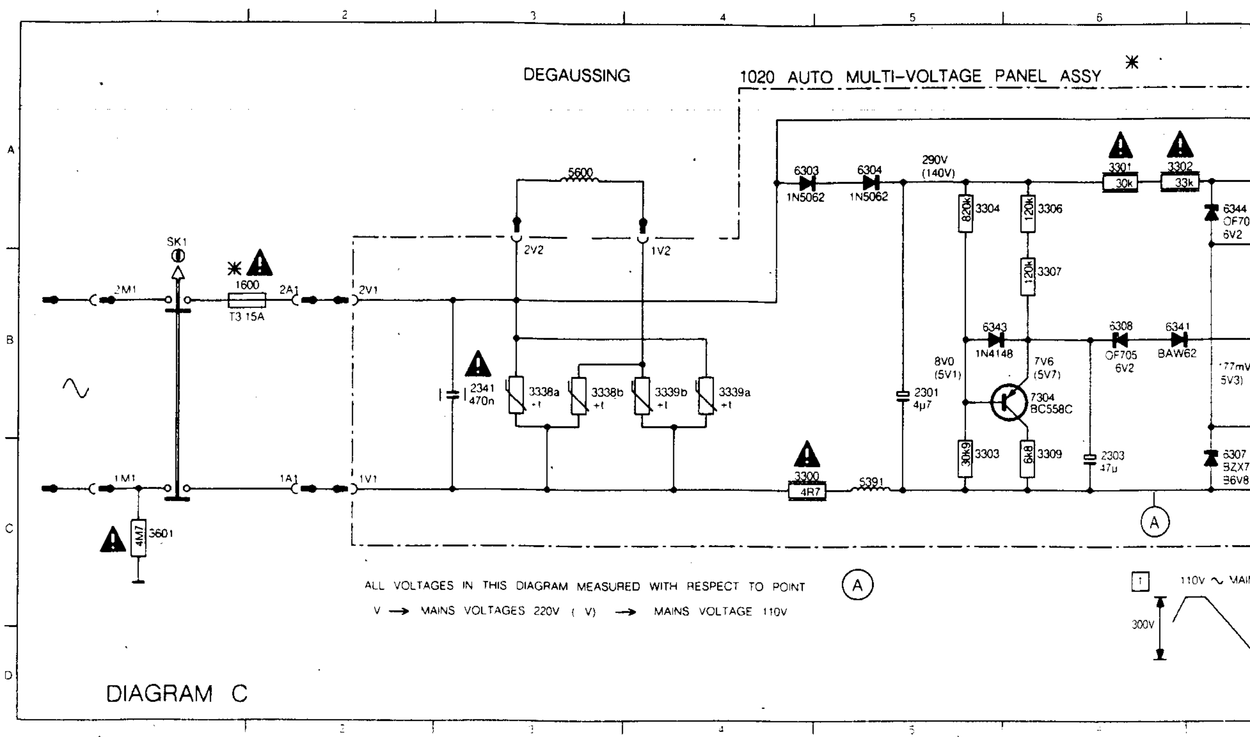


Fig. 2-

3 VST–4 OPERATING SYSTEM

3.1 Introduction

The VST–4 (Voltage Synthesis Tuning) operating system is based on the principle that tuning to a transmitter in the unit is done by varying linearly the varicap voltage for the channel selector.
The central part of the VST–4 system is a microcomputer which processes the operating commands, the analogue control voltages and takes care of tuning.
The system has the capacity to store 40 personal preference channels with their tuning and band voltage in a program memory. Using an OSD (= **O**n **S**creen **D**isplay) generator, information is given regarding the tuned band, position in the tuning range (tuning bar), program number, sleep timer and setting of the analogue controls.
There are 4 analogue controls available: volume, brightness, contrast and colour saturation, for which a certain setting can also be preprogrammed in a memory as personal preference (PP).
Sound suppression (mute) takes place during tuning to a transmitter or when interrupting a transmitter signal. The whole system is operated by an infrared remote control with RC5 command code or by a local operating unit on the equipment.

3.2 Block diagram (fig. 3.1)

The central part of the operating system is a 42–pin C–mos microcomputer (IC7840) of the type TMPC47C434.
In order to ensure that the microcomputer starts from an initialised state, as soon as the unit is switched on a Power On Reset signal (RESET) should first be given on pin 33.
During this RESET signal the internal oscillator of the microcomputer starts. The frequency of the oscillator (4 MHz) is set using a crystal or a resonator (1779) on pins 31 and 32.
The RC5 operating code, coming from the infrared remote control receiver U1785, is available on pin 35.
The operating unit is scanned using pins 10 to 14.
For tuning the channel selector the microcomputer gives a pulse–width modulated (PMW = Pulse–width modulated) signal at pin 1, from which an integrating network that operates as a D/A convertor builds up the tuning voltage Vvari.
Using the AFC switch TS7786, pin 41 ensures that during tuning the AFC control voltage originating from the MF detector (IC7020-A) has no effect on the Vvari. The AFC voltage is measured on pin 9.
The binary code for the band in which tuning takes place is on pins 17 and 18. IC7750 (LA7910) makes a 1 out of 4 code from this binary code, which directly operates the band selection of the channel selector.
During tuning the microcomputer ensures that the volume on pin 2 is set to minimum (Silent tuning).
The transmitter recognition signal (coincidence) comes in on pin 16. This becomes high if a transmitter has been found and then the microcomputer switches the sound on again.
Pins 2,3,4 and 5 supply pulse–width modulated signals which are converted by D/A converters into analogue control voltages for volume, brightness, colour saturation and contrast, respectively. Using pins 39 and 40 which are the clock (SCL) and data (SDA) line respectively (together forming the I^2C bus), the memory is controlled.

3.3 Switching unit on (see appendix 2).

As described in section 2.2.7, after the unit has been switched on with the mains switch, the supply voltage is present, which means that a RESET pulse is generated. This starts the oscillator in the microcomputer. After the RESET pulse the microcomputer starts with the initialisation.

During the initialisation the following take place one after the other:

- The internal RAM is tested.
  If a fault is found, error message FO is given using the LED 6757 (see section 3.12).
- The presence of the non–remote option diode (between pin 14 and 10) is checked. If the diode is present, the unit cannot be put to standby.
- The presence of a diode between pin 14 and 11 is checked. If the diode is present, only the UHF band will be selected.
- The presence of a diode between pin 14 and 12 is checked. If the diode is present, when the unit is switched on it will start with program 2 (used for units for Australia).
- The internal dividers and timers as well as the RC5 input are released. From this moment operating commands can be given.
- The last system status is read. If the status was standby, then the unit will be in standby.
- The working stores of the analogue controls are given the personal preference values.
- The internal timers of the microcomputer are tested. If they are not working properly, error message F1 is shown (see 3.12).

3.4 Local keyboard

The local keyboard has the facility to connect 9 keys arranged in a matrix of 3 columns and 3 rows. The keyboard is scanned every 16.4 msec. For this the pins 10, 11 and 12 are first made high ("1") and then a check should be carried out to establish whether one of the pins 11, 12 or 13 is low. This means then that one of the keys "store", "control up" or "program plus" has been pressed. Pin 10 then becomes low, it should be checked whether one of the keys "control min", "menu" or "volume plus" has been pressed. If no key has been pressed, proceed immediately to make pin 11 low and then pin 12. If a key has been found, scanning stops and the function is put in the memory. After one second the µC tries to read in the command again. This prevents the switches rattling.

3.5 Tuning

The microcomputer has 40 fixed locations to store program data. In these locations 14 bits are reserved for generating a pulse–width modulated signal to build up the tuning voltage.
The pulse–width modulated signal becomes available on pin 1. The period time of the pulse–width modulated signal is 8192 µsec.
Because the tuning voltage must be able to go up to 30V and the output level of the microcomputer does not supply this voltage, a resistor network (3703,3704 and 3705) is controlled with transistor 7705. Because this resistor network is powered from the 33V supply voltage, at the junction of R3710, R3703 and R3704 there is a pulse–width modulated signal with a maximum level of approx. 30V.
Via an integrator network consisting of R3710 and C2710 and ripple filter R3711 and C2711, a controllable tuning voltage Vvari (from 0–30V) is now built up for the channel selector.

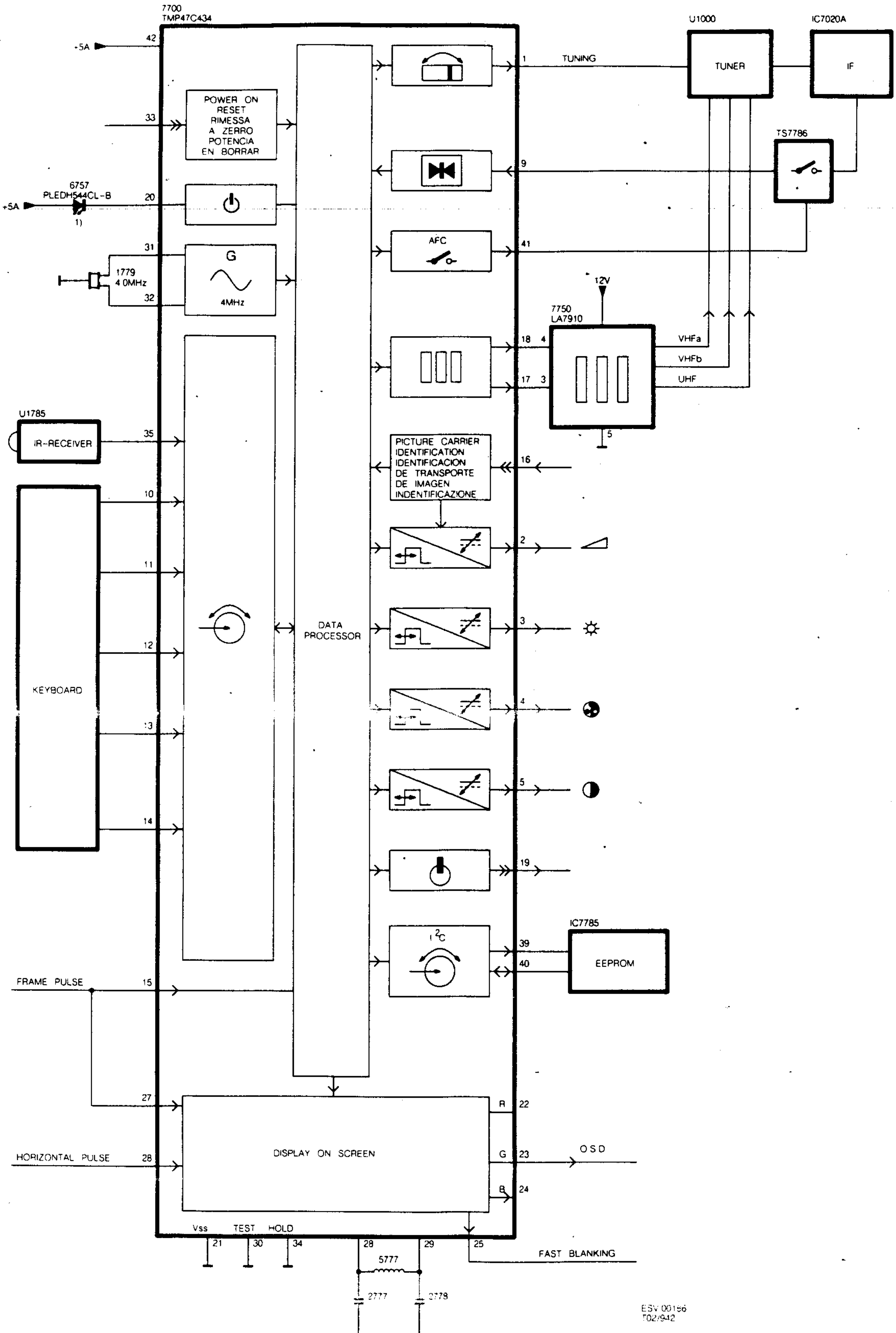
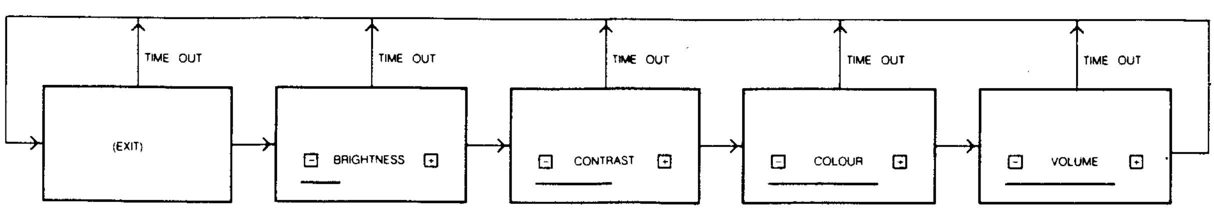


Fig. 3-1



"MENU" FUNCTION

Fig. 3-2

3.6 A.F.C.

For correcting the tuning voltage using the AFC control voltage (Vafc) the microcomputer has two connecting pins, one of which is used as an output and the other as an input.

- pin 9
  This continuously measures the AFC control voltage. The control voltage is supplied in the microcomputer to two comparators. One comparator obtains a reference voltage of 2.55V, while the other is supplied with 4.24V. Thus 3 voltage areas can now be identified on pin 9: <2.55V, 2.55–4.24V and >4.24V.
  Because resistor network R3730, R3731 divides the voltage, for the AFC control voltage the following areas apply: <4.5V, 4.5–7.5V and >7.5V. The microcomputer uses the AFC control voltage on pin 9 during the automatic fine tuning and just after a program switchover command.
- pin 41
  This pin is used as an output and ensures that the AFC control voltage has no effect on the adjustment during tuning via switching transistor 7786.

3.7 Automatic tuning

Automatic tuning can be started by first pressing the "store" and then the "control up" key.
The tuning bar then appears on the screen to indicate where the tuning is in the tuning range.
If automatic tuning is started, pin 2 of IC7700 becomes "low" so that the sound is suppressed. Moreover, the effect of the AFC voltage is eliminated by making TS7786 conductive. This transistor starts to conduct, so that on the collector there is a voltage of 6V. This is the nominal value for the Vafc.
The contents of the 14–bit tuning register are now quickly increased with the result that the duty cycle of the pulse–width modulator, from which the tuning voltage is derived, also changes. As soon as a video signal is recognised by the identification circuit in IC7020–B, the "IDENT" signal becomes high. The output of pin 41 of the µC becomes low again, so that the AFC can be measured once more. The µC continues to tune at an accelerated rate until V_{AFC}=4.5V. The fine tuning then starts. The tuning voltage is slowly increased until V_{AFC}=7.5V. It is then adjusted back until V_{AFC} is approximately 6V. During fine tuning the tuning voltage is only adjusted a limited number of steps, because it may be the case that "IDENT" has become high as a result of an interference signal or an incorrect video signal. If in the meantime the "IDENT" signal has become low again, the µC will continue to tune automatically.
If the tuning voltage has come to the end of the band, it switches over to the next band. The switchover takes place using IC7750. This IC obtains the band information in binary form and ensures that the correct band is switched.
As soon as it has tuned to a transmitter, the program number under which the located transmitter must be stored can be entered.

3.8 Program selection

3.8.1 Storing the program information

The tuning information in the 14–bit tuning register of the microcomputer, together with the band information (2 bits) is stored in an internal 16–bit memory of the microcomputer, after the store procedure has been completed.
Each program number has a fixed location.
The store procedure is carried out on the command of the local control and is as follows:

- After the tuning has found a required transmitter, a flashing line appears on the screen to indicate that the tuning information present at that moment can be stored in the memory.
- Using the program selection key, select a program number under which the program information is to be stored. This number then flashes.
- Then press the store key, so that the tuning information for the location belonging to that program number is stored.

3.8.2 Program selection (Program step)

The program step function (+ or –) is carried out using the remote control of the keyboard. By using this function, the user can sequentially select all programs, beginning with the program most recently selected.
When the highest (39) or the lowest (0) number is reached, there is automatic switchover to the lowest or highest program number, respectively.
If the "program step" key is pressed when the unit is in the standby mode, the TV will switch on with the last program shown. If the TV is switched on with the mains switch, the first program shown is always program 1 (except versions for Australia where this will be program 2).

3.8.3 Tuning after program switchover

During switchover the microcomputer will carry out the following:

- suppress the sound,
- switch off the AFC loop,
- fill the working stores with tuning and band information from the corresponding program memory and pass these to the corresponding outputs,
- start the fine tuning procedure and check whether the transmitter recognition signal is present.

3.8.4 Fine tuning

The Vafc is checked after each program change. If this is not approximately the nominal value (between 4.5 and 7.5V), one attempt is made using a slow tuning procedure to obtain optimum tuning.
If this is successful, the new value is automatically stored in the program memory.
Variation of the channel selector is automatically corrected using this procedure.

3.9 Analogue controls

The control of volume, brightness, contrast and saturation takes place in a set sequence in a menu (see fig. 3.2). By pressing the menu key, the brightness first appears on the screen and this can then be set using "control up" or "down".
The microcomputer has four 6–bit "working stores" available for the analogue settings which can be controlled in 64 stages from maximum to minimum.
On the pins 2,3,4 and 5 there is a pulse–width modulated signal with a repetition time of 32 µsec and the duty cycle is dependent on the contents of the working stores.
The control rate of the analogue functions is determined by the internal software timer in the microcomputer and the time from minimum to maximum is approximately 7 sec.
Direct voltages are generated by the pulse–width modulated signals via integrator networks.
Volume, brightness, colour saturation and contrast are minimum at an output level of 0V and maximum at 5V.

Notes:

If the sound if suppressed using the mute key (which becomes visible on the screen), the sound is switched on by a volume +/– command or by pressing the mute key again.

3.10 Personal preference

The preference positions of the 4 analogue controls can be stored in the internal memory of the microcomputer. For this the personal preference should first be set (in the menu) and then the store execute key pressed.
When the unit is switched on, the contents of the personal preference memories are transferred to the working stores.

3.11 Timer function (⏻)

The microcomputer also has a "sleep timer". This can only be switched on using the remote control. When this function is switched on, the unit goes to standby after a set time. The maximum time is 90 minutes and this can be reduced in steps of 15 minutes by pressing the timer key.

3.12 OSD function (On Screen Display)

This gives the following functions on the screen (in green):

- set values for the analogue controls
- program number
- timer information
- a search bar so that it is possible to see where the tuning is.

The OSD generator is synchronised by a vertical flyback pulse via pin 27 and with the sandcastle pulse via pin 26. Using these signals the correct place for displaying information on the screen can be determined. The frequency for the OSD generator (approximately 5 MHz) is determined by the LC network between pin 28 and 29. The output signal of the generator is at pins 23 and 25. Pin 23 supplies the information for a letter (or a line) which must be shown. Pin 25 is used to suppress the TV signal at the place where the OSD information is visible.

3.13 Automatic switching off (only for units with standby)

The microcomputer looks every 50 msec to see whether there is a video signal present on pin 16 of IC7700 (the identification signal). If there is no longer a video signal, a counter is started and after 10 minutes the unit is switched to standby. The counter is of course reset to zero as soon as a signal is recognised or when a command is given (using the keyboard or the remote control).

3.14 Hotel mode

The microcomputer also has a hotel mode which is only intended for use in hotels. By pressing a combination of keys, this mode can be activated. A number of functions are then blocked:

- It is no longer possible to store a transmitter. If the "store" key is pressed, nothing happens.
- It is no longer possible to change a personal preference setting. Care must be taken with the sound, as in the hotel mode the sound cannot be set louder than it was set previously using the preference setting.
- If the unit is in the standby mode and the p+ or p– key is pressed, the unit will start with program 1 instead of the most recently selected program.

The hotel mode can be switched on by first selecting program 38 and pressing the "store" and p+ at the same time. (Here the "store" key should be pressed first and then the p+ key).
The hotel mode can be switched off by selecting program 38 once more and then pressing the "store" key and control+ key at the same time.

3.15 Error messages

3.15.1 Introduction

The VST4 operating system can generate 3 error messages (F0 to F7). These error messages are displayed using a flashing LED. The on time of the LED is always 50 ms. The off time depends on the error message (see table 3.1).

error message	off time (ms)
F0	50
F1	100
F2	150

3.15.2 Explanation of the error messages

F0: Internal RAM fault
If during the initialisation a fault is discovered in the RAM of the microcomputer, FO is generated and the TV will stop working.

F1: Internal timer fault
The timers of the microcomputer are checked during the initialisation. If there is something wrong, F1 is generated.

F2: EEPROM fault or +5B not present
If when reading or writing to the EEPROM no confirmation is received, F2 is generated.

4. THE CHANNEL SELECTOR AND IF CIRCUIT

4.1 Channel selector

Figure 4.1 gives a block diagram of the VHF + UHF channel selector. The VHF_a bandswitch voltage is applied to pin 7 and the VHF_b bandwitch voltage to pin 8. The UHF bandswitch voltage is fed to pin 10.
The tuning of the RF amplifier and the oscillators is determined by the tuning voltage that is fed to pin 11. This tuning voltage can originate from any control system and is correctedby the AFC voltage.
After mixing of the oscillator and the RF signal the IF signal is formed which is amplified and fed to outputs 16 and 17.
If an UV7.. or U743 is applied then pin 16 is connected with earth, because this range has an assymetric output.
The UV6.. range is also used and this has a symmetric output.
The AGC voltage at pin 5 controls the amplification of the RF amplifiers.

4.2 IF amplifier and demodulator (enclosure 1)

The IF output signal of the channel selector present at pin 16-17–U1000 is fed to the SAW (Surface Acoustic Wave) filter U1030. The SAW filter provides the correct IF band pass. The IF signal at the output of the SAW filter is applied to the input of the IF amplifier/detector IC7020–A pins 8 and 9.
In this IC the IF signal is first amplified and is then applied via an overload detector to a balance demodulator. The reference signal needed for demodulation is obtained via U5045, which is exactly tuned to the picture carrier.
By demodulation the luminance signal is formed, the colour and sound information superposed on it. These signals are fed via an amplifier stage to pin 17.
In the IC the demodulated video signal is also fed, via a low–pass filter, to an AGC (Automatic Gain Control) circuit. This circuit supplies a DC voltage, which is dependent on the average value of the video signal. With this DC voltage the amplification of the IF amplifier is controlled. Thus a video signal is generated at the output the amplitude of which is practically independent of the amplitude of the IF signal applied.
If the video signal exceeds a specified value, the AGC circuit also provides a delayed AGC voltage. This delayed AGC voltage is fed to the VHF and UHF amplifier in the channel selector. In this way overdrive of these amplifiers is prevented. The threshold value of the delayed AGC circuit can be adjusted with potentiometer R3021.

The AFC (Automatic Frequency Control) circuit in IC7020–A is supplied with two signals: the reference signal, which is first shifted 90°, and the carrier wave of the video signal.
The frequency at which the phase is shifted 90° is determined by the tuning of reference circuit U5045 which is also exactly tuned to the picture carrier frequency.
The AFC circuit supplies a DC voltage, the value of which is determined by the phase difference (frequency) of the two signals applied (picture carrier and reference signal).
The resulting AFC voltage, which is present at pin 18–IC7020–A, is fed via voltage devider R3730/R3731 to pin 9 of microcomputer 7700. Now correct tuning is performed via the microcomputer. A voltage coming from the coincidence circuit in IC7020–B is fed to the AFC circuit in IC7020–A. This voltage turns the AFC circuit off during tuning, because automatic frequency control is undesirable during tuning. For the functioning of the AFC, see chapter 3.6 AFC.

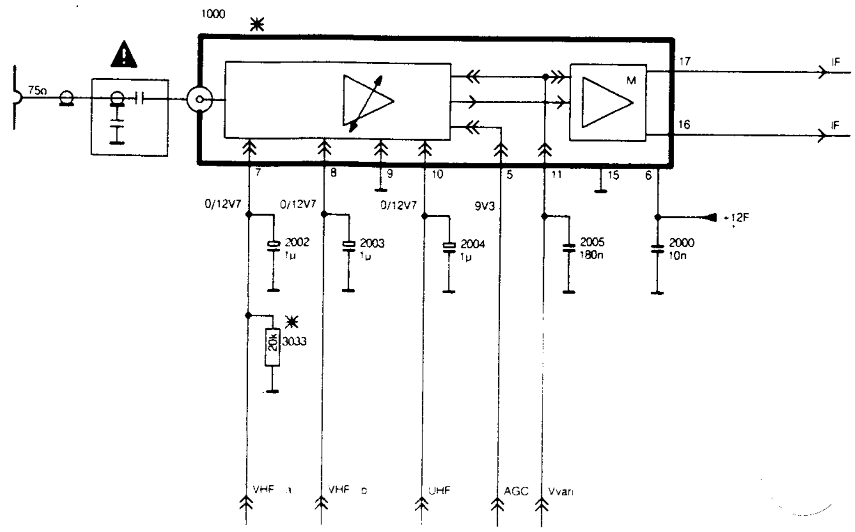


Fig. 4.1

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5. LUMINANCE AND CHROMINANCE CIRCUIT

5.1 Luminance circuit

The circuit is built up around IC7300 (TDA3565). The video signal which is present on pin 17 of IC7020–A is applied via network S5040, TS7040, R3038, U1038, R3324, U1326 R3327 and C2328 to pin 8 of IC7300. In this network, U1038 is used for suppressing the sound intermediate frequency and U5602 for delaying (330 nsec) the brightness signal in relation to the colour signal. This delay is necessary because the colour signal passes through an extra band–pass circuit with small bandwidth, as a result of which the colour signal gets a greater envelope delay time than the brightness signal. As the brightness signal and the colour signal have the same delay during their entire signal paths, they arrive simultaneously on the picture screen.
The brightness signal present on pin 8–IC7300 is amplified by a controlled amplifier. The gain is adjusted by the voltage on pin 6–IC7300, which is dependent on the contrast control 5–IC7700. The black level is determined by the voltage on pin 9–IC7300, which is dependent on the brightness control 3–IC7700. The voltage on pin 6–IC7300 (contrast setting) can also be influenced by the beam–current information. If the beam current becomes too great, diode 6551 will start conducting so that the voltage on pin 6–IC7300 decreases and hence also the contrast. The amplified brightness signal is then applied to the B–G–R matrices, in which the brightness signal is added to the colour difference signals.

5.2 Chrominance circuit

The video signal is fed via U1038, R3320-C2321, C2320, L5320 (band–pass filter for the colour signal) to pin 3 of IC7300.
The colour signal is amplified with a controlled amplifier, the gain of which is determined by:
- the DC voltage on pin 5–IC7300, which is determined by saturation control coming from 4–IC7700
- the output signal of the colour switch in IC7300.
- the output signal of the burst peak detector in IC7300 (H/2).
- the voltage on pin 6–IC7300, which is applied via the contrast circuit to the controlled amplifier.

The output signal present on pin 18–IC7300 is fed via C2300 and R3300 to PAL delay line U1303. Furthermore the output signal of pin 18–IC7300 is symmetrically added - via R3301, R3302 and C2302 - to the delayed signals on the output of delay line U1303.
The phase is set between the delayed signal and the direct signal by means of L5303. The ratio between the amplitudes of the direct and delayed signals is set by means of R3302.
So the input signal for the B–Y and R–Y demodulators is the sum of the colour signal of a line plus the colour signal of the preceding line.
The B–Y and R–Y demodulators are synchronous demodulators which receive their reference signals via a crystal oscillator which is synchronized with the burst signal.
This oscillator works at twice the frequency (8.86 MHz) of the burst signal (4.43 MHz). The oscillator frequency is divided by two and then forms the reference signal for the B–Y demodulator. This reference signal is also fed to the PAL switch. Every other line the reference signal for the R–Y demodulator is rotated 180° in phase by the PAL switch. Depending on the phase of the burst signal received, the phase of the R–Y reference signal is either the same or is given an extra 180° phase shift. In this way the reference signals for +(R–Y) and –(R–Y) are formed.

The crystal oscillator is synchronized with the burst signal. To this end the phase of the crystal oscillator is compared by means of a phase detector with the phase of the burst signal received. The burst signal which is present in the colour signal on pins 13 and 14 of IC7300 is used for this.

The output signal of the phase detector is dependent on the phase relation between the signals applied and is used to correct the phase of the crystal oscillator.
The network at pin 15–IC7300 determines the time constant of the phase detector, and furthermore the free–running frequency of the crystal oscillator can be adjusted by means of R3313. The time constant is so great that the average phase of the burst signal is followed.
In a second phase detector (H/2) the phase of the burst signal is compared with the phase of the H/2 flip–flop. Depending on the phase of the burst signal, this flip–flop is either set or reset to bring the PAL switch in the right position.
If the burst signal is too weak or if it is not present at all, or if the H/2 flip–flop is in the wrong position, the B–Y and R–Y demodulators are turned off via the colour switch, so that the colour reproduction is suppressed. The signals present on the outputs of the B–Y and R–Y demodulators are fed to the B and R matrices and also to the G–Y matrix.
In the G–Y matrix the B–Y and R–Y signals are added in the proper proportions, resulting in the G–Y signal which is added to the G matrix.
The output signals of the B–G–R matrices are applied to the B–G–R pre–amplifiers.
The sandcastle signal which is fed to this pre–amplifier is responsible for the vision suppression during line and frame flyback.
The output signals of the B–G–R pre–amplifiers are available on pins 12, 11 and 10 of IC7300 respectively, and are fed via L–C networks to the B–G–R amplifiers on the picture tube panel.

6.SECAM PAL/TRANSCODER

Sets equipped with a SECAM/PAL transcoder U1020 offer the possibility of demodulating apart from PAL also SECAM signals.
The transcoder, see Fig. 6.1, converts incoming SECAM signals into a PAL signal which is then supplied to the already present PAL demodulator.
The demodulated video signal that is present on the emitter of TS7040 is supplied via connector 2M7 to the SECAM/PAL transcoder.

6.1 Signal path for SECAM reception.

The video signal is supplied, via C2316, R3316 and filter S5316, to pin 3 of IC7310. Filter S5316 is tuned to the average frequency of the two SECAM colour carriers viz. 4.328 MHz.
Next the signal is amplified in block A, limited and then demodulated SECAM by block B.
Demodulator B is a FM demodulator; circuit S5347 forms part of this demodulator and is tuned to the average frequency of the two SECAM colour carriers (4.328 MHz).
Block B supplies three output voltages:

- the demodulated R–Y signal;
- the demodulated B–Y signal;
- an identification signal for the SECAM/PAL identification block. The SECAM/PAL identification block is dealt in 6.3.

During the line flyback demodulator B is blocked by a line pulse passed on from block W and via block D.
In blocks K and L the detected R–Y and B–Y signals are every other line clamped at a defined DC voltage level and supplied to block M.
The above-mentioned process is controlled by the output signal of the H/2 flip-flop, block H, thus switching electronic switches V and M in the correct positions.
If the switches are in the drawn mode during one line, the R–Y signal is clamped and passed on via M; the B–Y signal is blocked then.
During the next line H changes state and V and M assume the non-drawn mode. Now the B–Y signal is clamped and passed on; the R–Y signal is blocked.
The composite signal, at the output of block M, is via blocks N and P supplied to PAL encoder block R.
In block N the deemphasis takes place and higher harmonics of the SECAM subcarrier frequencies are filtered out while in block P the BURST signal is added.
In block R the R–Y and B–Y signals are modulated in the correct (PAL) way on a 4.43 MHz subcarrier (supplied by block Q) and then the modulated signals are available at pin 9 of IC7310.
Finally, these signals are via R3336, R3335, C2335 supplied directly to the PAL matrix, block U, and via C2337, R3337,U1337, C2338 delayed one line duration and also passed on to the PAL matrix.
The PAL matrix, block U, combined the direct and the delayed signal which results in a PAL modulated chroma signal which is via switch T present at pin 14 of IC7310.
Next this signal is supplied to the chrominance input of IC7300 (CHROM./LUM. circuit).

The video signal is also via R3320, U1320, R3322 and C2321 supplied to pin 16 of IC7310. The luminance signal present at this point is amplified in block S.
The output signal of block S is available at pin 15 of IC7310 and is supplied to the luminance input of IC7300 (CHROM./LUM. circuit).

6.2 Signal path for PAL reception.

If the SECAM/PAL transcoder is fed a PAL signal, switch T will be in the PAL mode.
Then the SECAM decoding and the PAL encoding, as described in 6.1 are switched off.
The signal present at connector 2M7 is via R3320, U1320, R3322 and C2321 supplied to pin 16 of IC7310 and next it is amplified in block S. In case of PAL, block S supplies two video signals: one is available at pin 15 of IC7310 and is supplied to the luminance input of IC7300 (CHROM./LUM.circuit); the other signal is available at pin 14 of IC7310 and is supplied to the chrominance input of IC7300

6.3 SECAM/PAL identification.

The SECAM/PAL identification is based on the assumption that the received signal is a PAL signal and the transcoder is thus switched in the PAL mode.
The voltages at pins 6 and 7 of IC7310 are high then. If a BURST signal is present in the transmitter signal, the colour killer in CHROM./LUM. demodulator IC7300 gives a high level (>1.7V) which via connector 1M7 is passed on to pin 13 of IC7310.

The voltage at pin 13 of IC7310 thus goes high causing the voltage at pin 6 of IC7310 to remain high. Consequently, the transcoder maintains the PAL mode.
If no BURST signal is present, the colour killer gives a low signal. Consequently the voltage at pin 13 of IC7310 is low, which causes pin 6 of IC7310 to go low as well. Not until some time later the voltage at pin 7 of IC7310 also goes low. In this way is achieved that the identification is not affected all kinds of interferences.
The transcoder will assume the SECAM mode if moreover the SECAM identification signal is also detected by block B. Both line and frame identification takes place.
To this end two signals are supplied to the LINE/FRAME identification block E:

- one complete sync signal for frame identification from block W.
- one pulse supplied by block F which has been delayed 0.8 µsec. relative to the trailing edge of the BURST key-out pulse (BK).

Frame identification takes place at the moments the identification signal is present during the frame flyback.

After the transcoder has identified a SECAM signal, it converts the SECAM signal into a "quasi" PAL signal.
Now the colour killer in IC7300 again supplies a high signal because once again a BURST signal is present in the PAL signal. As a result the transcoder would again assume the PAL mode!
This undesired phenomenon is automatically prevented in IC7310: once the SECAM/PAL transcoder is in the SECAM mode, this mode is maintained as long as the transmitter signal is present.

Various blocks in IC7310 are fed control signals that have been derived from the sandcastle pulse. This pulse is coming from the sync circuit. Here one should think of blocks E, F, V, M and P.
These signals are obtained from block W which is via pin 19 of IC7310 fed the sandcastle pulse. It is decomposed in three signals:

- a BURST key-out signal (BK);
- a horizontal sync signal (H);
- a composite sync signal (H+V).

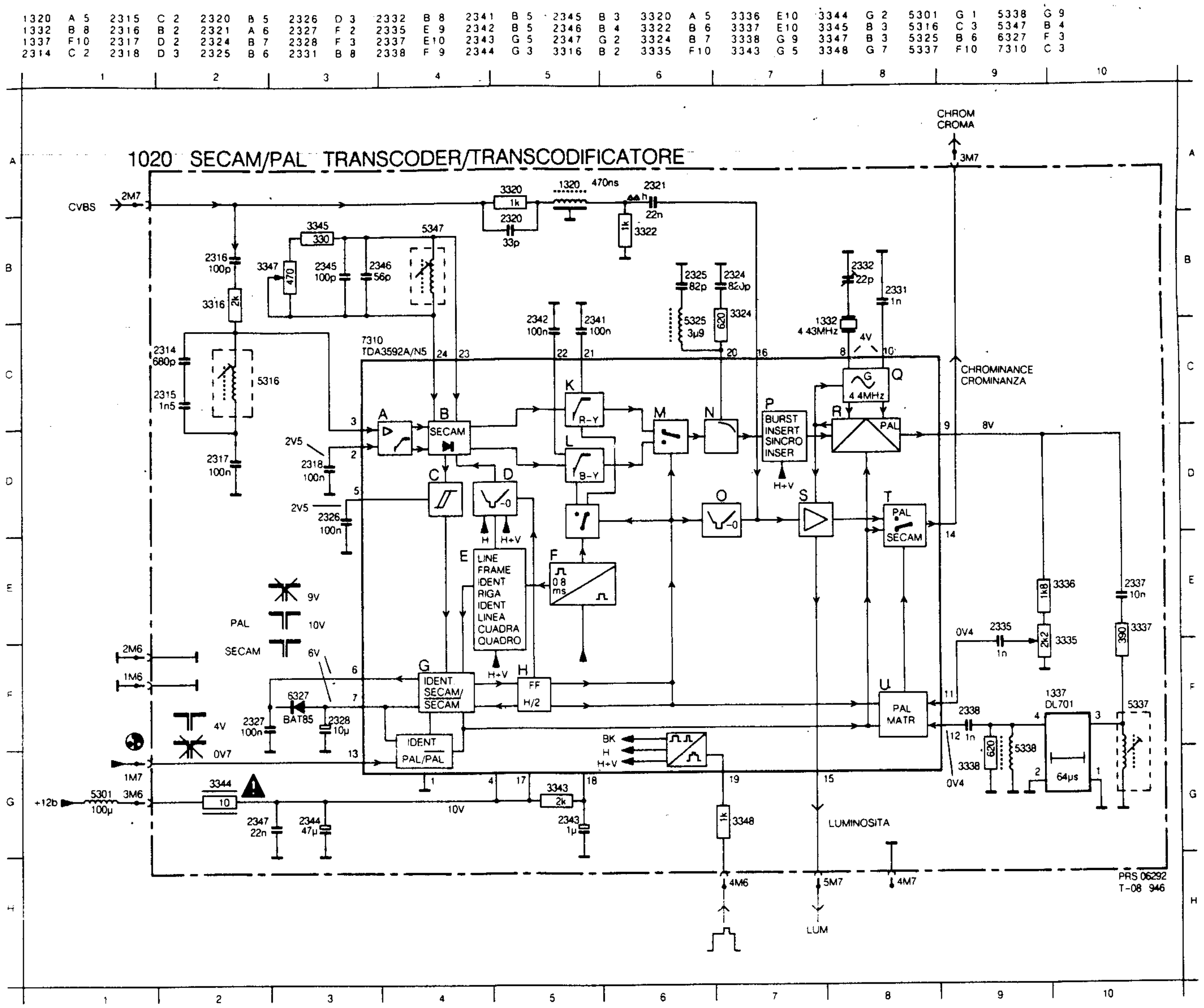

Fig. 6-1

1320	A 5	2315	C 2	2320	B 5	2326	D 3	2332	B 8	2341	B 5	2345	B 3	3320	A 5	3336	E10	3344	G 2	5301	G 1	5338	G 9
1332	B 8	2316	B 2	2321	A 6	2327	F 2	2335	E 9	2342	B 5	2346	B 4	3322	B 6	3337	E10	3345	B 3	5316	C 3	5347	B 4
1337	F10	2317	D 2	2324	B 7	2328	F 3	2337	E10	2343	G 5	2347	G 2	3324	B 7	3338	G 9	3347	B 3	5325	B 6	6327	F 3
2314	C 2	2318	D 3	2325	B 6	2331	B 8	2338	F 9	2344	G 3	3316	B 2	3335	F10	3343	G 5	3348	G 7	5337	F10	7310	C 3

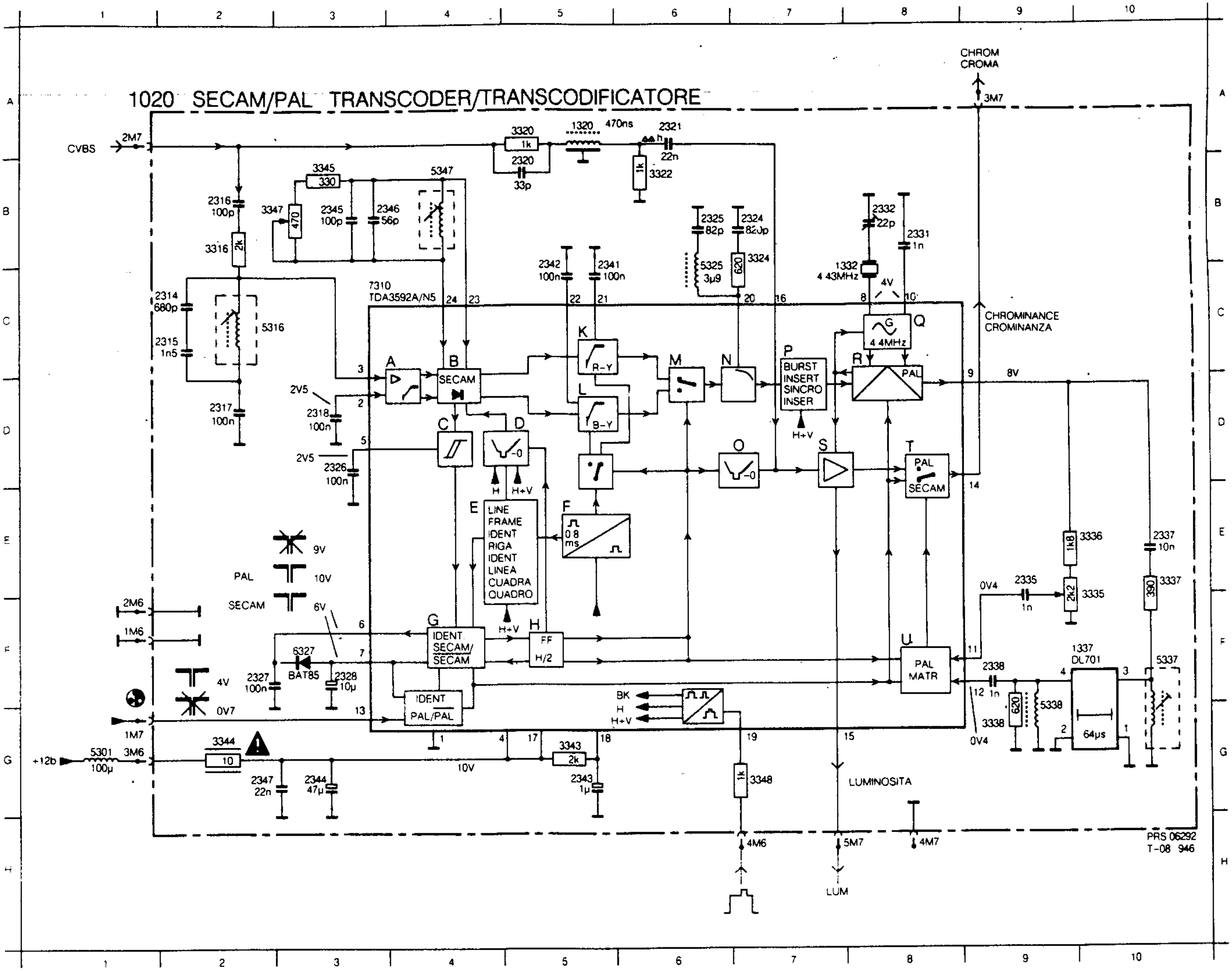

Fig. 6-1

7. B-G-R AMPLIFIERS

The B-G-R amplifiers are situated on the picture tube PCB. As these amplifiers are all identical, only the R amplifier will be described.
The DC setting of TS7415 is partly determined by TS7402. As a result of voltage division of the +12B supply voltage via R3400 and R3401, the base voltage of TS7402 is 2.4V. Consequently the emitter voltage of TS7402 is 3.1 V.
The DC voltage on pin 10 of IC7300 varies depending on the brightness control.
The voltage on point 5 of the CRT-panel is set at 3.1 V with the brightness control. In this situation no current flows through R3409, so that no basecurrent flows to TS7415. The collector voltage of TS7415 is now set at 125 V with R3412.
The VG2 control is now adjusted such that the light on the picture tube screen just disappears. This is done for the colour which disappears first. For the other two colours R3412, R3422 and/or R3432 should be adjusted slightly until the picture tube is just dark for all three colours.
With this the cut-off points of the picture tube are set. The advantage of the circuit applied is that no changes in background colour occur as a result of temperature influences or drift of the +12B supply voltage.
The RC network R2414, R3414 compensates the reduction in gain at the higher video frequencies, so that the largest possible bandwidth is obtained.
Resistor R3440 protects the circuit against the adverse consequences of voltage flash-over in the picture tube.
With trimming potentiometers R3421 and R3431 white balance is adjusted at high picture brightness.

8. SOUND CIRCUIT

The IF sound signal which is present in the demodulated video signal on pin 17-IC7020-A is fed via L5040, C2037, ceramic filter 1036/1037 and C2036 to pin 15 of IC7020-C. The ceramic filter has been tuned to the sound intermediate frequency, so that only this frequency is passed.
The signal is fed via pin 15-IC7020-C to an amplifier, in which the signal is symmetrically limited. Any amplitude modulations on the signal applied are thus effectively suppressed.
After amplification, the signal is applied to a balance demodulator. The reference signal for the demodulator is obtained via parallel circuit L5034, L5035, C2033, which is connected through C2033 to pin 13-IC7020-C. This circuit is exactly tuned to the sound intermediate frequency.
After demodulation the LF signal obtained is fed to a controlled LF pre-amplifier. The control voltage for this pre-amplifier is obtained via microcomputer 7700 in the control unit. (See chapter 3.9 analogue controls).
The amplified LF signal which is present on pin 12-IC7020-C is fed via R3032, C2032, C2102, R3102, R3103 and C2103 to the 1W output amplifier IC7103 (TDA7052). This an amplifier of 1W whitch is supplied with 10V (+9A) from the BUCSO-supply.

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9. SYNCHRONISATION CIRCUIT

9.1 Starting the synchronisation IC

This is possible via pin 11 of IC7020-C. This pin has a double function:

- volume control
- starting the synchronisation.

When the unit is switched on, there is a power supply of 97.5V. This voltage charges C2058. The capacitor which is still empty is charged and the voltage pulse which for a short time is on pin 11 of IC7020-C starts up the line oscillator. The current which then flows in the IC should not be too great (8.5mA max.). The voltage peak is thus limited by D6030 to 12V. Via TS7521 and TS7523 the line oscillator now started provides the line transistor TS7528 with the control pulses required. The 12V supply voltage is now produced from the line output stage, which is supplied via pin 7 to the IC7020-C. Various supply voltages are produced by the line output stage which is now working.

9.2 Sync separator

If tuning to a transmitter has taken place, a video signal will be present at pin 25 of IC7020-B.
This signal contains picture information and sync signals. R3052 and C2052 ensure that the unnecessary picture information at pin 25-IC7020-B is attenuated.
The sync separator at this pin only allows sync pulses to pass.

9.3 Horizontal synchronization and oscillator

The horizontal oscillator contains a free-running sawtooth generator. Its free-running frequency is by means of R3049 adjusted for the line sync frequency.
During adjustment of the R3049 the input (pin 25) should be connected with pin 7 (+12A).Across capacitor C2048, which forms part of this oscillator, a sawtooth voltage develops.
The horizontal oscillator is synchronised with the transmitter signal by means of a control voltage coming from the phase-1 detector.
To this end the phase-1 detector is supplied with two signals:

- via the gate, the transmitter sync signal
- the fed back oscillator signal.

With the control voltage that is generated in the process the horizontal oscillator is adjusted via the time constant switch and the network between pins 23 and 24.
The control time constant is affected by the time constant of circuit R3051, C2050, C2051 and the time constant switch.
When the set is out of synchronization, the gate is kept conducting as long as possible, so that as many sync pulses as possible can be supplied to the phase-1 detector, to quickly lock-in a transmitter.
When synchronisation has taken place, the gate will only briefly be conducting.
In this situation it is an information signal of the coincidence detector (transmitter identification signal) which selects via the time constant switch a time constant which is optimal for VCR playback. If a transmitter with weak signal is received, a greater time constant will be selected to improve picture stability.
Because accurate timing of the burst key signal is required, a sawtooth signal from the horizontal oscillator is used for this purpose.
The burst key generator passes the burst key signal plus the line pulses on to the sand castle generator.
Together with the vertical blanking signal the sand castle signal is generated now.
Now the sand castle signal at pin 27 contains appart from the line pulses and the burst key signal also the vertical blanking information.

To ensure that the horizontal output signal at pin 26-IC7020-B is synchronous with the sand castle signal, the phase-2 detector has been applied.
This detector is affected by R3054 so that the horizontal centring can be corrected.

9.4 Vertical synchronization and control stage

From the output signal supplied by the sync separator the vertical sync separator delivers the vertical sync pulses. These pulses are supplied to a divider.
This divider has an internal frequency doubler circuit by turning each pulse coming from the horizontal oscillator, into two clock pulses. These clock pulses are counted.
The counter is reset by the vertical sync pulse.
If the next vertical pulse arrives before line 576, the system works in the 60 Hz mode.
If the pulse arrives later, the 50 Hz mode is selected.
Because the output pulse of the divider is triggered by the first clock pulse after the vertical sync pulse, no vertical frequency adjustment needs to take place.
Together with the negative-feedback signal coming from the frame output stage, at pin 4-IC7020, and the signal from the divider the vertical oscillator and the vertical driver are driven.
The RC network at pin 2-IC7020 is only used as edge generator.
The signal which is now present at pin 3-IC7020, is used to drive the frame output stage.

10. THE FRAME OUTPUT STAGE (fig. 10.1)

The frame output stage in IC7500 (TDA3653) is driven by the driver stage in IC7020-B.

During the scan the supply voltage of + 26 V is sufficiently great to obtain the required current intensity through the deflection coil. During flyback, however, the variation in current per unit of time is much greater, so that the selfinductance of the deflection coil now starts to play a role. The + 26 V supply voltage is no longer sufficient. A higher voltage is required and this is provided by the flyback generator, which works as follows:
During the scan pin 8 of IC7500 is maintained at 0 V. Capacitor C2515 is charged to a voltage of + 26 V. During the flyback the flyback generator gives a voltage pulse of + 26 V on pin 8 of IC7500. At pin 6 a voltage pulse of + 52V is formed, being the + 26 V of pin 8-IC7500 plus the + 26 V of C2515. As a result diode D6516 is blocked. Since the flyback at the output is slower than at the input because of the self-inductance of the deflection coil, a negative voltage pulse is formed at pin 1 (IC7500) during the flyback. This voltage drives the frame output stage to full power so that the maximum voltage of 50 volts occurs at the output. The current strength through the deflection coil is now sufficiently great to see to the flyback.

The output amplifier contains a protection circuit which keeps the dissipation within limits and a thermal protection which switches the circuit off when the temperature of the IC exceeds 175° C.
The IC also contains a supply voltage stabilizer which keeps the voltage constant despite the high load current. The shape of the output voltage is now such that a sawtooth will flow through the vertical deflection coil.
When there is no deflection current and the flyback generator is not activated, the voltage at pin 8 reduces to less than 2 V. A protection in IC7500 will then produce a d.c. voltage at pin 7, which is used to blank the picture tube and thus prevents screen damage.
A sawtooth shaped voltage is formed across R3511/R3512. Via R3510 and R3507 this voltage is fed to pin 4 of IC7020. With R3510 the amount of feedback, and thus the vertical amplitude can be adjusted.
A parabola shaped voltage is formed across C2504. Part of this voltage is integrated by R3505 and C2505. Via R3506 this correction voltage is fed to pin 4 of IC7020 thus providing "S"-correction.
Resistor R3502 and C2502 are applied across the deflection coil to damp the line-frequent voltages in the deflection coil, so that no line-interlace faults occur.

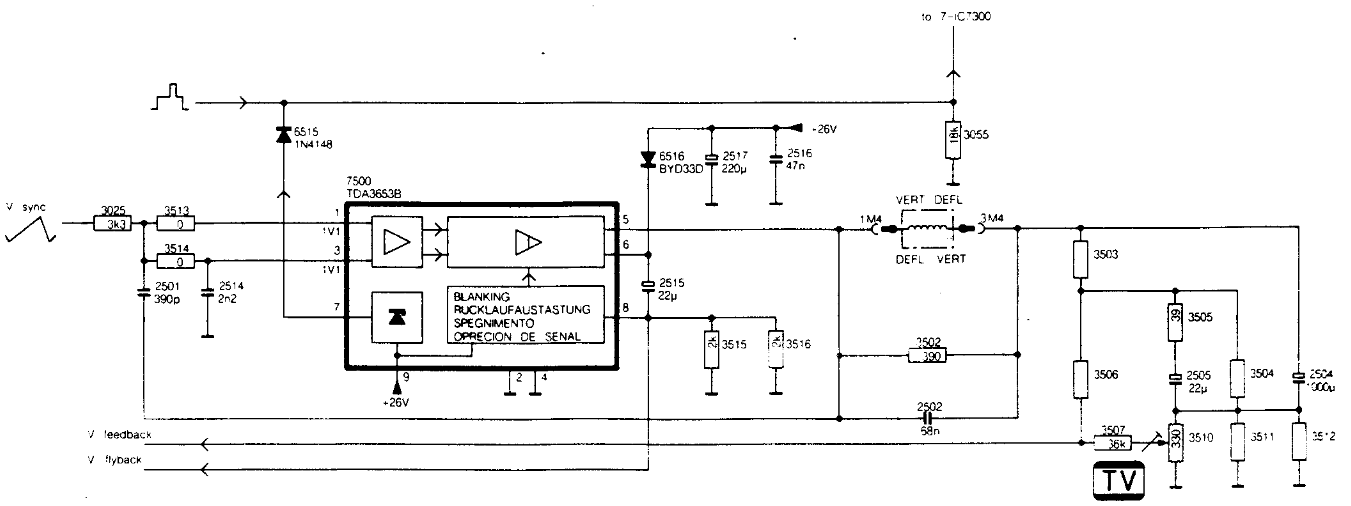

Fig. 10-1

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11. LINE OUTPUT STAGE

The line output stage supplies:

- the deflection current for the horizontal deflection coils
- the supply voltage for the picture tube
- the +160 supply voltage that is used to supply the RGB amplifiers in the set.
- blanking signals.
- various voltages that are used for supply various circuits in the set

11.1 Line driver and horizontal deflection circuit

The control voltage for the line driver is taken from pin 26 of IC7020-B, the sync IC, and is via L5519, R3520/L5521 and R3500 supplied to the base of TS7521.

The working of the line output stage is explained on the basis of the simplified circuit of 9.1, together with the wave shapes of the fig. 11.2.

Capacitor C2 is via the primary winding of T5520, L in fig. 11.1, raised to a voltage of approx 100 volts. The voltage across C2 remains virtually constant since C2 has a high capacitance.
During t1–t2 the control voltage at the base of TS is positive, causing this transistor to conduct.
Coil L has now been switched parallel to C2, resulting in a constant voltage across coil L.
Consequently, a linearly increasing current starts to flow through L and TS (I_L and IC_{ts}, during t1–t2 in fig.11.2).
At moment t2 the control voltage at the base of TS becomes negative, causing the transistor to switch off.
The current which flowed through L, flows on through L C1, thus bringing energy from L to C1. The current through L drops and the voltage across C1 rises sinusoidally.

In time t_3 all energy from L has been transferred to C1 and energy recovery starts during t_3–t_4. Now C1 feeds current back to L so that the voltage across C1 drops and the current through L is sinusoidal. If all energy from C1 were now again transferred to L the voltage across C1 would want to become negative.
At moment t4 the voltage at the cathode of D wants to become negative causing D to conduct.
There once again is a constant voltage present across coil L and as a result a linearly increasing current starts to flow through the coil (t4–t6 in fig.11.2).
Current I_L goes from maximum negative to zero (moment t5) and then the current direction reverses. Now diode D is blocking but because the base current of TS has just before moment t5 become positive again the transistor conducts again and current I_L is again flowing through TS as of moment t5. At moment t5 the same situation as at moment t1 has developed.

As described before, the control voltage of TS (V_{in}, see fig. 11.2) becomes positive before moment t5 has arrived.
As of the moment V_{in} becomes positive up to moment t5 – the hatched part of V_{in} – the transistor starts to conduct.
Part of the current through D during t4 to t5 is flowing through the transistor, see fig. 11.3. The transistor is conducting inversely here.

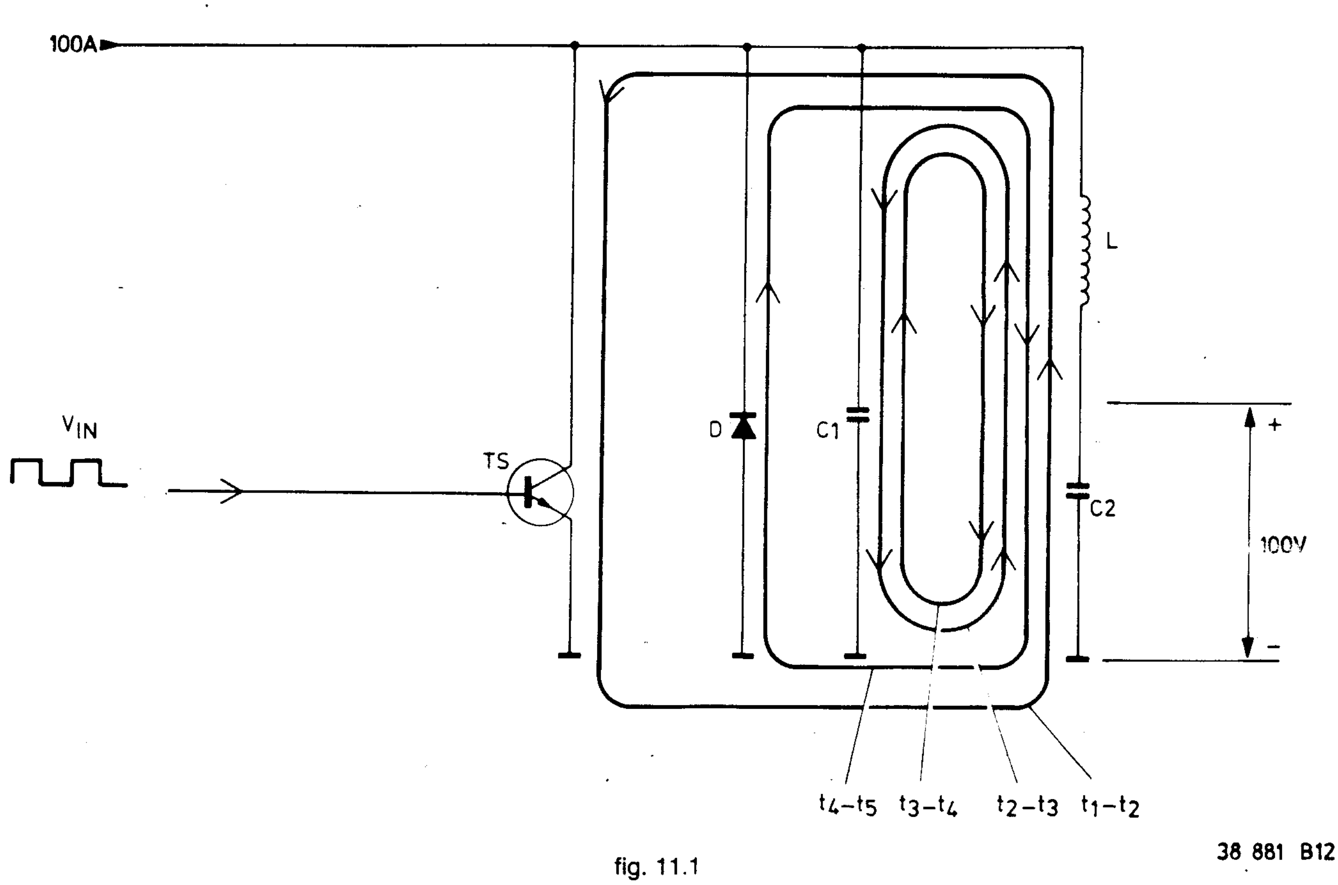


fig. 11.1

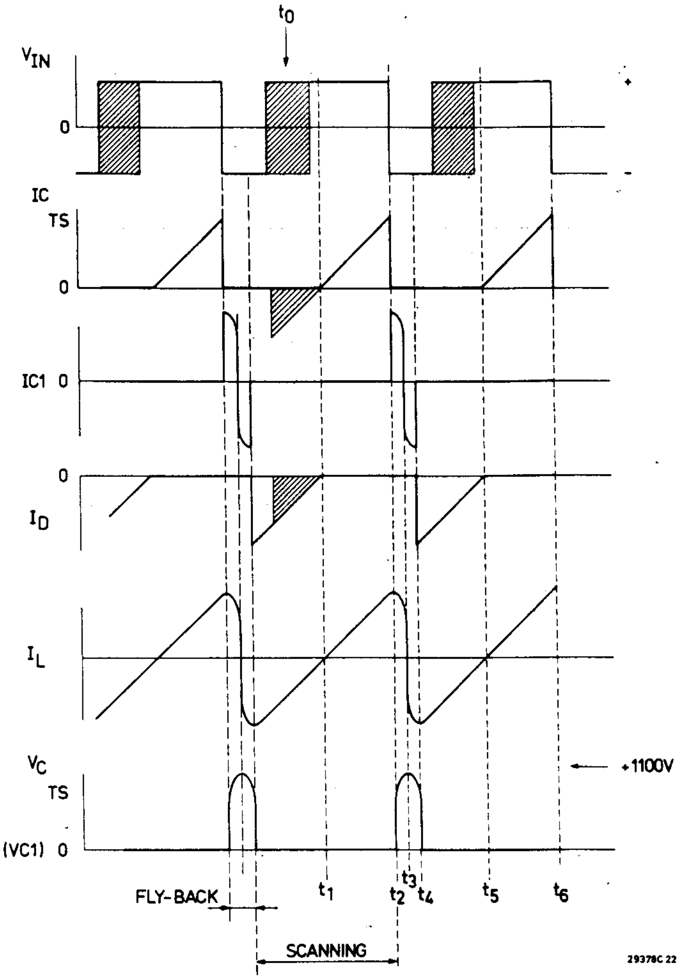


Fig. 11.2

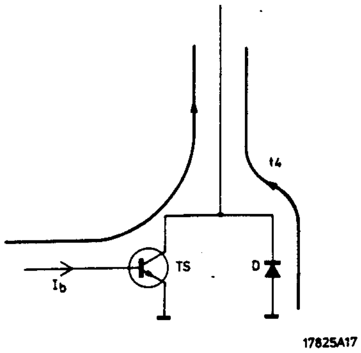


Fig. 11.3

The description is based on the assumption that the capacitance of C2 is infinitely great. In that case the current through coil L is really purely linear. However, a purely linearly increasing deflection results in a linearity error on the picture because the picture screen is part of a circle, whose centre does not coincide with the centre of the deflection coils: the picture screen is too flat.
To offset the occurring linearity error the capacitance of C2 is not infinite, causing the deflection current to undergo an S-shaped distorsion, see fig. 11.4.

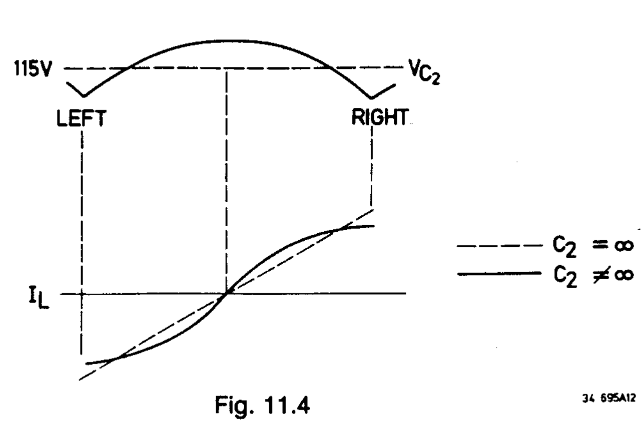


Fig. 11.4

11.2 Generation of the power supply voltages for the picture tube

The picture tube circuit, see fig. 11.5, is supplied the following high voltages:
- the 25 kV high voltage
- the focussing voltage
- the VG2 voltage

The various voltages are obtained through rectification of the line flyback pulses that are present across the secondary of T5530. Here use has been made of a series of diodes that each rectify part of the voltage. This way of switching is called the diode-split method. All diodes have been accomodated in the secondary winding (co-wound). The diode-split method works as follows:
The voltage that develops across winding a–b is rectified with D1 and smoothed with C1. The resultant DC voltage is supplied to the lower side of winding c–d.
The voltage across winding c–d is rectified with D2 and smoothed with C2. The voltage that results at cathode D2 is the sum of the voltages across C1 and C2.
The above is repeated for all windings and diodes in the transformer. The advantage of the diode-split method is that the voltage across each diode is relatively low.

The focussing voltage and the VG2 voltage are obtained from a tap on the secondary winding of T5530 and from the sliders of the FOCUS and VG2 potentiometers supplied to the picture tube. Both potentiometers are situated in the line output transformer.
The filaments of the picture tube are supplied from winding 9–8 of T5530.

11.3 Beam current limitation

The beam current for the picture tube flows from the +26 via R3550 and the secondary winding of T5530 to the picture tube.
The result across C2550 is a voltage that is the difference between the +26V and the beam current times the resistance value of R3550: as the beam current increases the voltage across C2550 decreases.
At a certain value of the beam current D6551 starts to conduct and as a result further increase of the beam current makes the voltage across C2342 lower. The luminance for the picture tube thus decreases because pin 6 is the contrast control point of IC7300, the chrominance/luminance IC.
In this way the beam current is limited to a maximum value.

11.4 Derived power supply voltage

The voltage that is present at pin 1 of T5530 is rectified by means of D6535 and smoothed with C2536.
The +160 power supply voltage that results across C2536 is used for supply of the RGB amplifiers in the set.
The voltage at pin 2 of T5530 is rectified by D6540 and used for the vertical output stage.
The voltage at pin 3 is rectified by D6542 to +12V.
Several 12V are built up to supply various parts in the television.

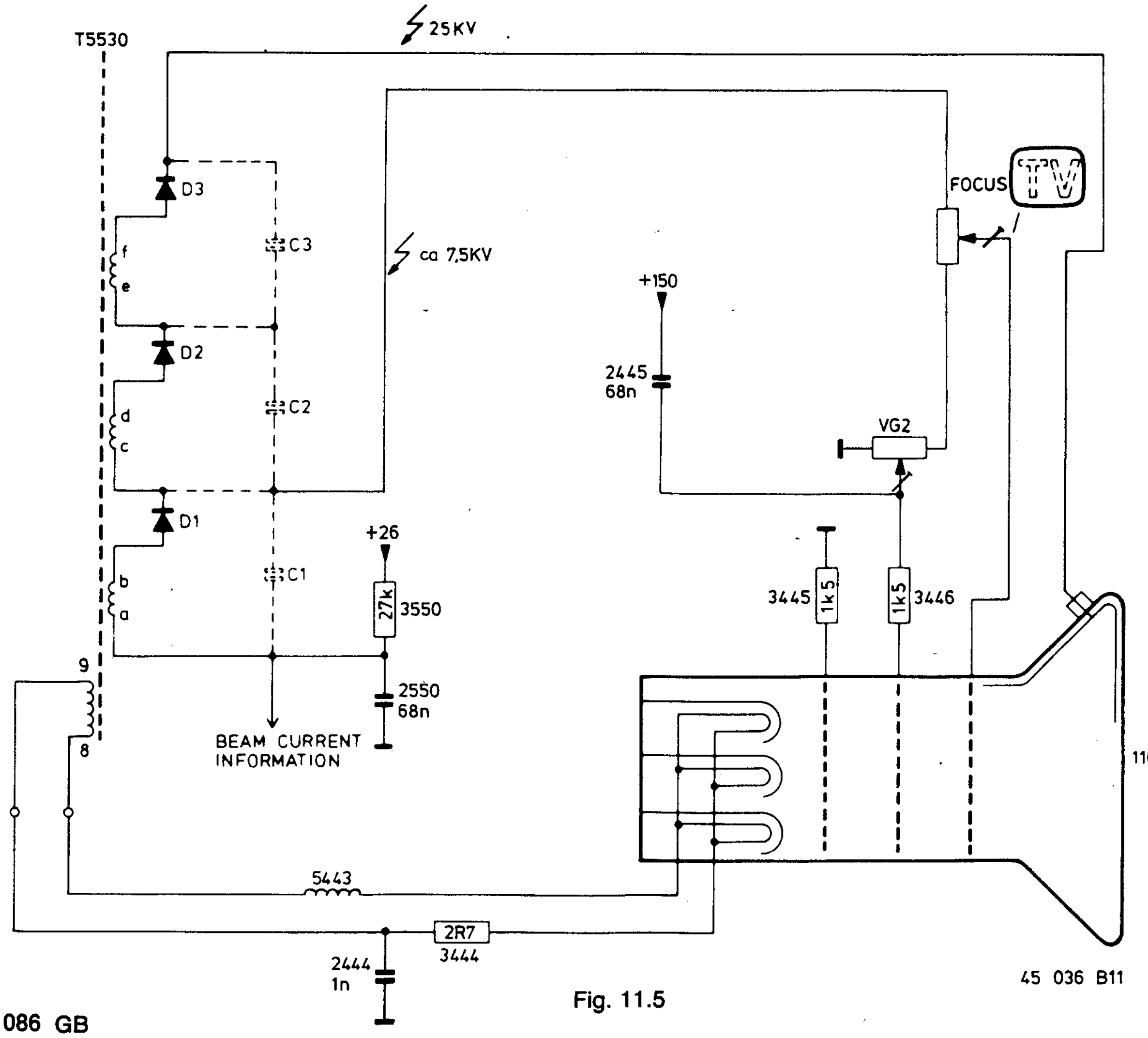


Fig. 11.5

12. CONVERGENCE

12.1 Static corrections

All these corrections are performed with magnetic rings in the so-termed "multipole unit".
This unit comprises two magnet rings for RED-BLUE convergence, two for Magenta-Green convergence and two for colour purity and vertical symmetry. The multipole unit is mounted on the back of the picture tube neck. Each ring of a set always comprises an equal number of magnet poles. The two rings of each set may be rotated arbitrarily relative to each other and also arbitrarily relative to the picture tube neck, so that any desired field strengt and any desired field direction can be obtained.

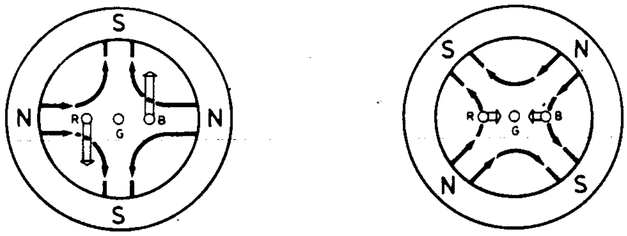


Fig. 12–1

12.1.1 Static convergence for red and blue

For this purpose two four-pole rings are employed. Fig. 12-1 clearly shows that the green beam is not influenced and that the red and the blue beam can be moved towards and away from each other. in other words, these four-pole rings enable the static convergence of the red and the blue picture.

12.1.2 Static convergence for magenta and green

For this purpose two six-pole rings are used (Fig. 12-2). Again the green beam is not influenced, but only the red and the blue beams in the same direction. This means that the magenta picture can be moved relative to the stationary green picture.

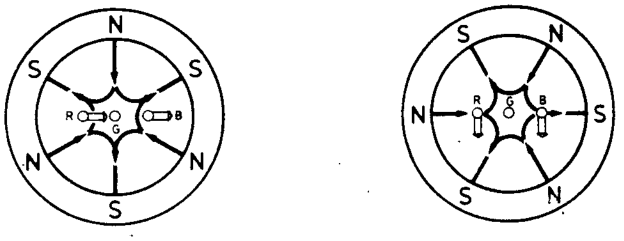


Fig. 12–2

12.1.3 Colour purity and vertical symmetry

For this purpose the unit comprises one pair of two-pole rings. Fig. 12-3 shows that if the field extends vertically, the three beams are shifted horizontally. This is the colour purity adjustment.
However, if the field extends horizontally, the three electron beams are shifted vertically, which results in a change in curvature of the central horizontal. This is the vertical symmetry adjustment. The rings should be adjusted so that they produce a field which contains the appropriate vertical and horizontal components, so that both the colour purity and the vertical symmetry are correct.

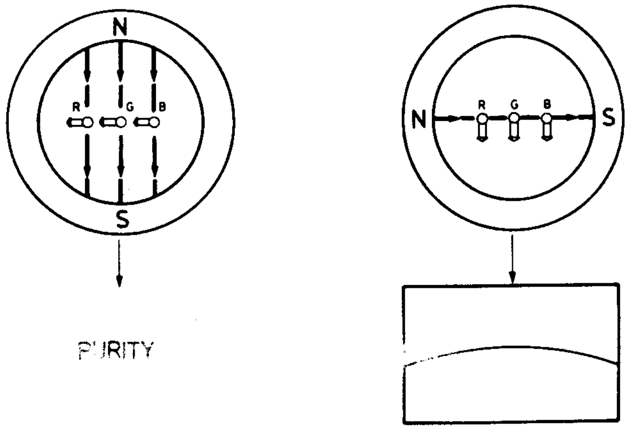


Fig. 12–3

12.2 Dynamic corrections

These corrections are realised by vertically and horizontally tilting the deflection unit.
The guns will then be situated in a slightly different field. The field distribution in the vertical deflection coil is as shown in Fig. 12-4 and that in the horizontal deflection coil as shown in Fig. 12-5.

The special distribution of the horizontal pin-cushion shaped and the vertical barrel-shaped deflection field renders the system self-converging. Moreover, the north-south distortion is very small owing to the barrel-shaped vertical deflection field, so that no correction for this is needed.

12.2.1 Horizontal tilting (Fig. 12-6)

The guns appear to be shifted along the horizontal axis. Either the red or the blue gun is then brought into a stronger deflection field. The dimensions of the red picture then, for example, increase, whilst the dimensions of the blue picture decrease. By a suitable choice of the horizontal tilting the picture dimensions can be equalised exactly.

12.2.2 Vertical tilting

Viewed in the vertical deflection field the R and B guns are situated in oblique field lines; so that the R and B beams are also subject to a certain amount of horizontal deflection. The blue vertical lines for example tilt clock-wise, whereas the red vertical lines are tilted anti-clock-wise (see Fig. 12-7)
Viewed in the horizontal deflection field the same happens so that the R and B beams are also subject to a certain amount of vertical deflection (see Fig. 12-8)
Summarising, this means that if the deflection coils are tilted vertically, the red picture is rotated relative to the blue picture. In this way the fault of Fig. 12-9 may be eliminated. After the appropriate horizontal and vertical tilting has been performed, the deflection unit is kept in position with rubber wedges.

vertical deflection

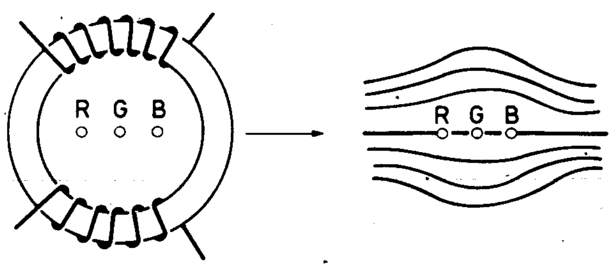


Fig. 12–4

horizontal deflection

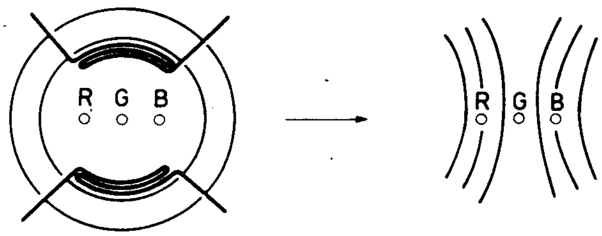


Fig. 12–5

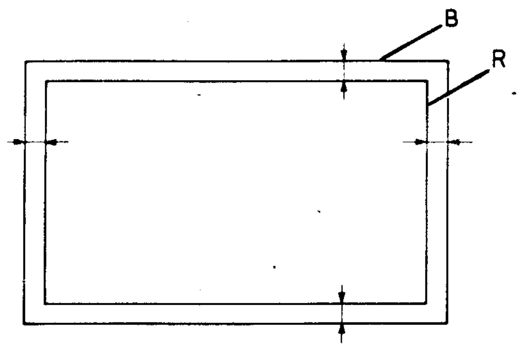


Fig. 12-6

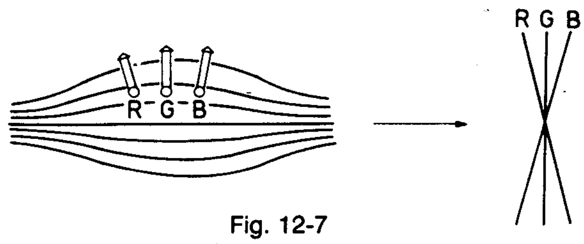


Fig. 12-7

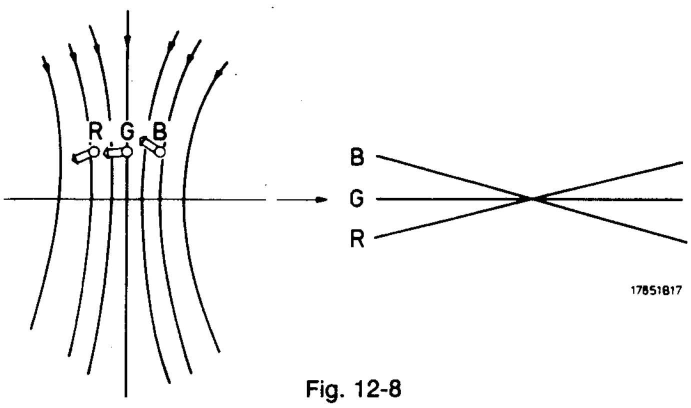


Fig. 12-8

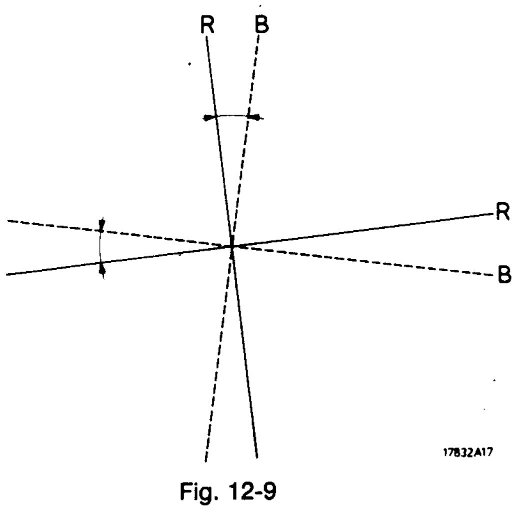


Fig. 12-9

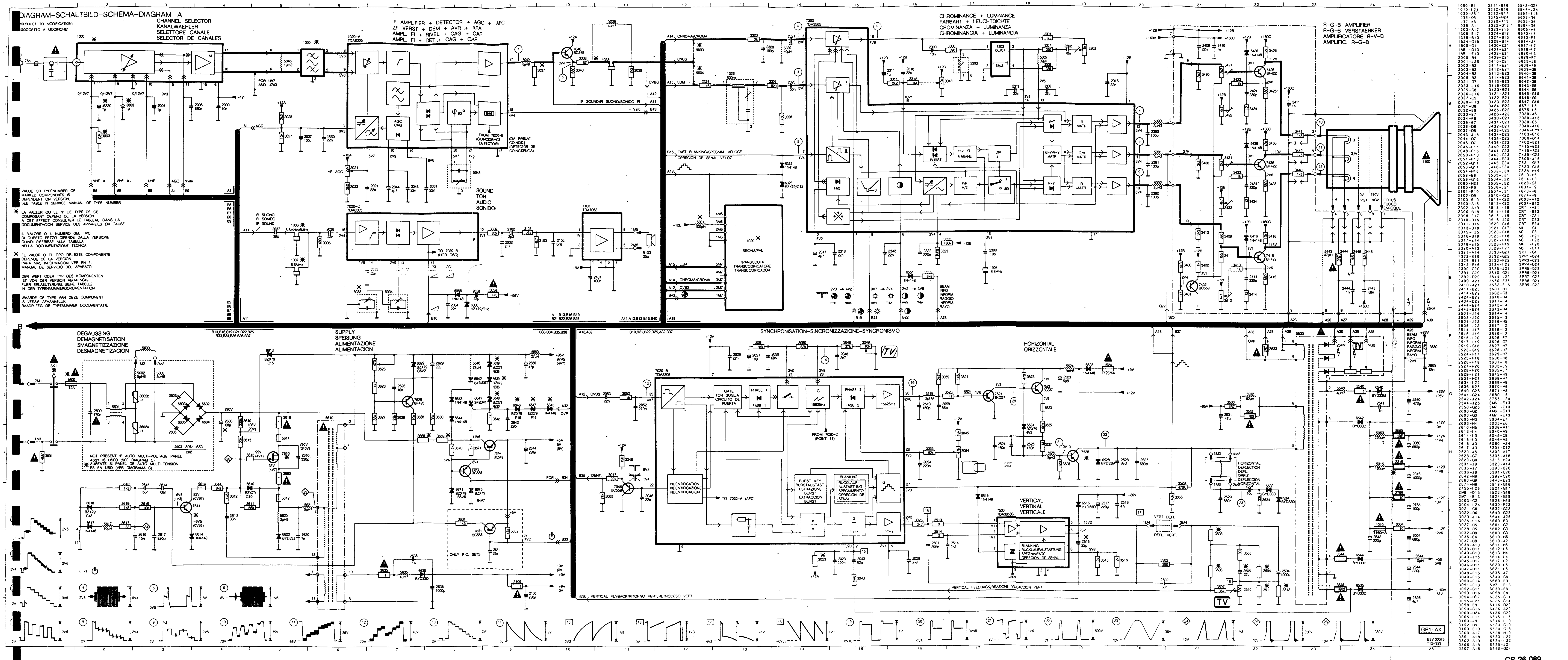


DIAGRAM-SCHALTBILD-SCHEMA-DIAGRAM A
(SUBJECT TO MODIFICATION)
(SOGGETTO A MODIFICHE)
CHANNEL SELECTOR
KANALWAEHLER
SELETTORE CANALE
SELECTOR DE CANALES
IF AMPLIFIER + DETECTOR + AGC + AFC
ZF VERST + DEM + AVR + AFA
AMPL. FI + RIVEL + CAG + CAF
AMPL. FI + DET. + CAG + CAF
CHROMINANCE + LUMINANCE
FARBART + LEUCHTDICHTE
CROMINANZA + LUMINANZA
CROMINANCIA + LUMINANCIA
R-G-B AMPLIFIER
R-G-B VERSTAERKER
AMPLIFICATORE R-V-B
AMPLIFIC. R-G-B
SOUND
TON
AUDIO
SONIDO
SECAM/PAL
TRANSCODER
TRANSCODIFICATORE
TRANSCODIFICADOR
DEGAUSSING
DEMAGNETISATION
SMAGNETIZZAZIONE
DESMAGNETIZACION
SUPPLY
SPEISUNG
ALIMENTAZIONE
ALIMENTACION
SYNCHRONISATION-SINCRONIZZAZIONE-SYNCRONISMO
HORIZONTAL
ORIZZONTALE
VERTICAL
VERTIKAL
VERTICALE
VERTICAL FLYBACK/RITORNO VERT/RETROCESO VERT
ONLY R.C. SETS
NOT PRESENT IF AUTO MULTI-VOLTAGE PANEL ASSY IS USED (SEE DIAGRAM C)
AUSENTE SI PANEL DE AUTO MULTI-TENSION ES EN USO (VER DIAGRAMA C)
VALUE OR TYPENUMBER OF MARKED COMPONENTS IS DEPENDENT ON VERSION. SEE TABLE IN SERVICE MANUAL OF TYPE NUMBER
GR1-AX

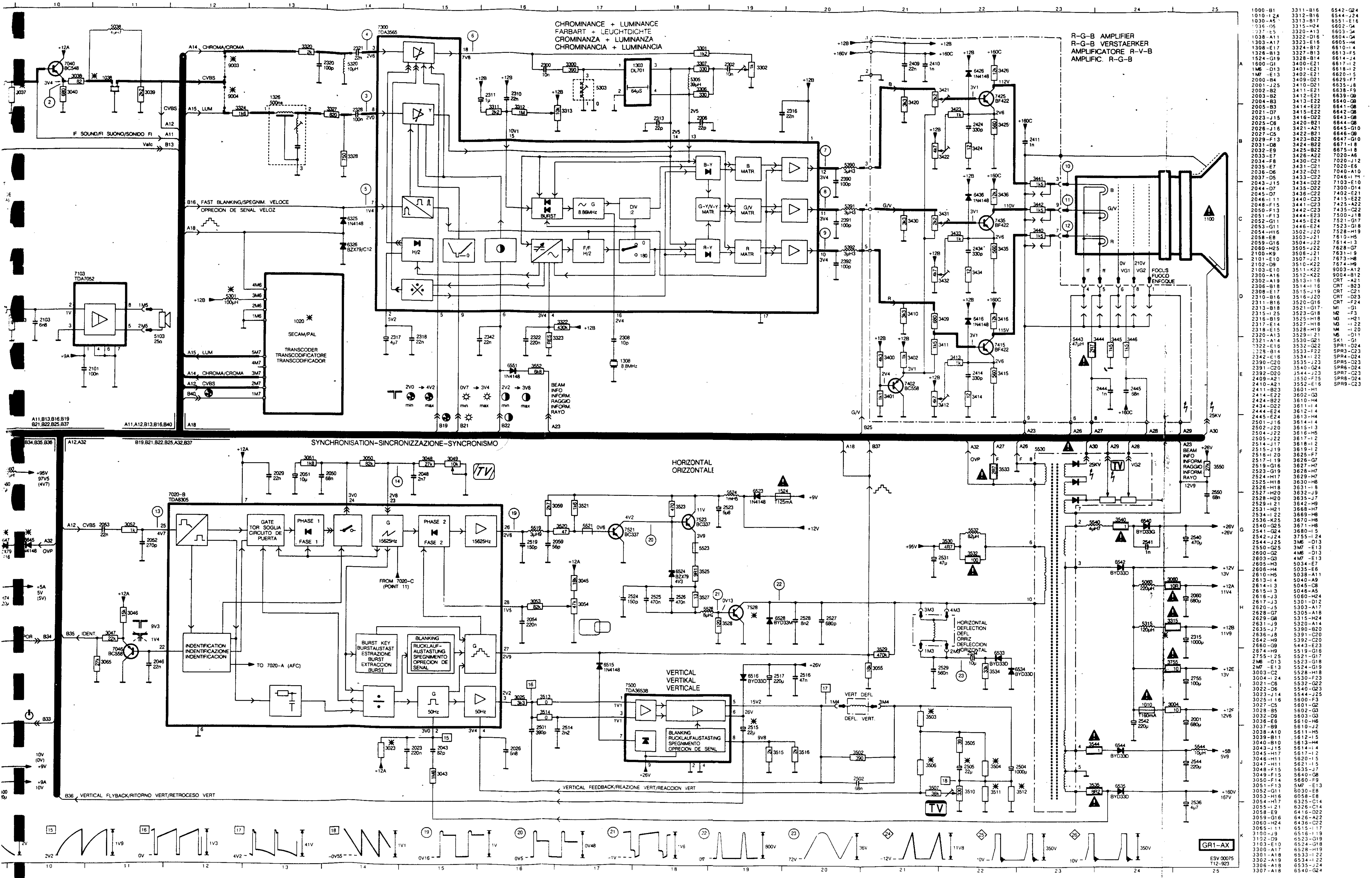
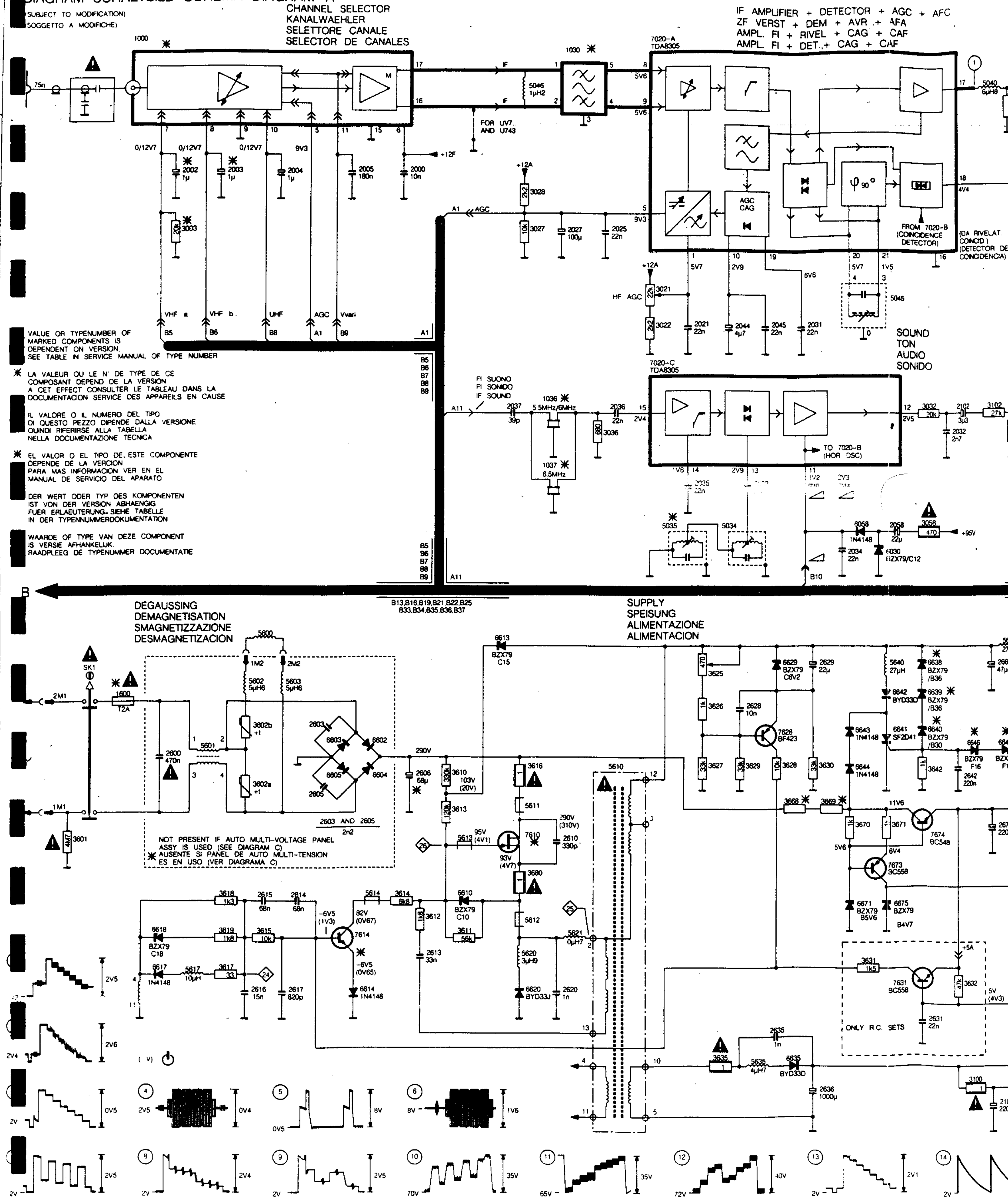
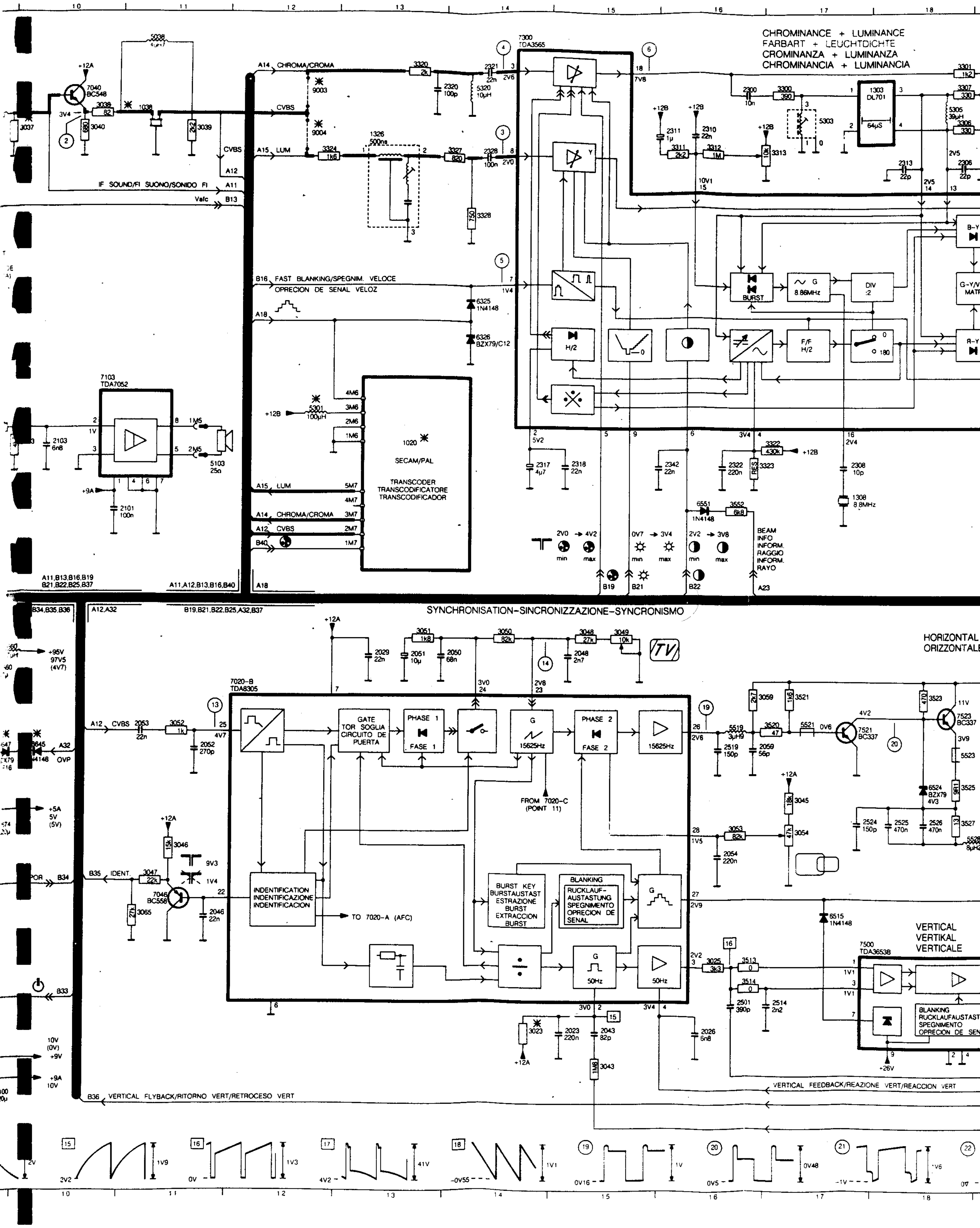

CHROMINANCE + LUMINANCE
FARBART + LEUCHTDICHTE
CROMINANZA + LUMINANZA
CROMINANCIA + LUMINANCIA
R-G-B AMPLIFIER
R-G-B VERSTAERKER
AMPLIFICATORE R-V-B
AMPLIFIC. R-G-B
SYNCHRONISATION-SINCRONIZZAZIONE-SYNCRONISMO
HORIZONTAL
ORIZZONTALE
VERTICAL
VERTIKAL
VERTICALE
7300 TDA3565
7020-B TDA8305
7500 TDA3653B
7103 TDA7052
1020 SECAM/PAL
TRANSCODER
TRANSCODIFICATORE
TRANSCODIFICADOR
IF SOUND/FI SUONO/SONIDO FI
B16 FAST BLANKING/SPEGNIM. VELOCE
OPRECION DE SENAL VELOZ
BEAM INFO INFORM. RAGGIO INFORM. RAYO
HORIZONTAL DEFLECTION
DEFL. ORRIZ
DEFLECCION HORIZONTAL
VERT DEFL
DEFL. VERT.
VERTICAL FEEDBACK/REAZIONE VERT/REACCION VERT
B36 VERTICAL FLYBACK/RITORNO VERT/RETROCESO VERT
GR1-AX
ESV 00075
T12-923

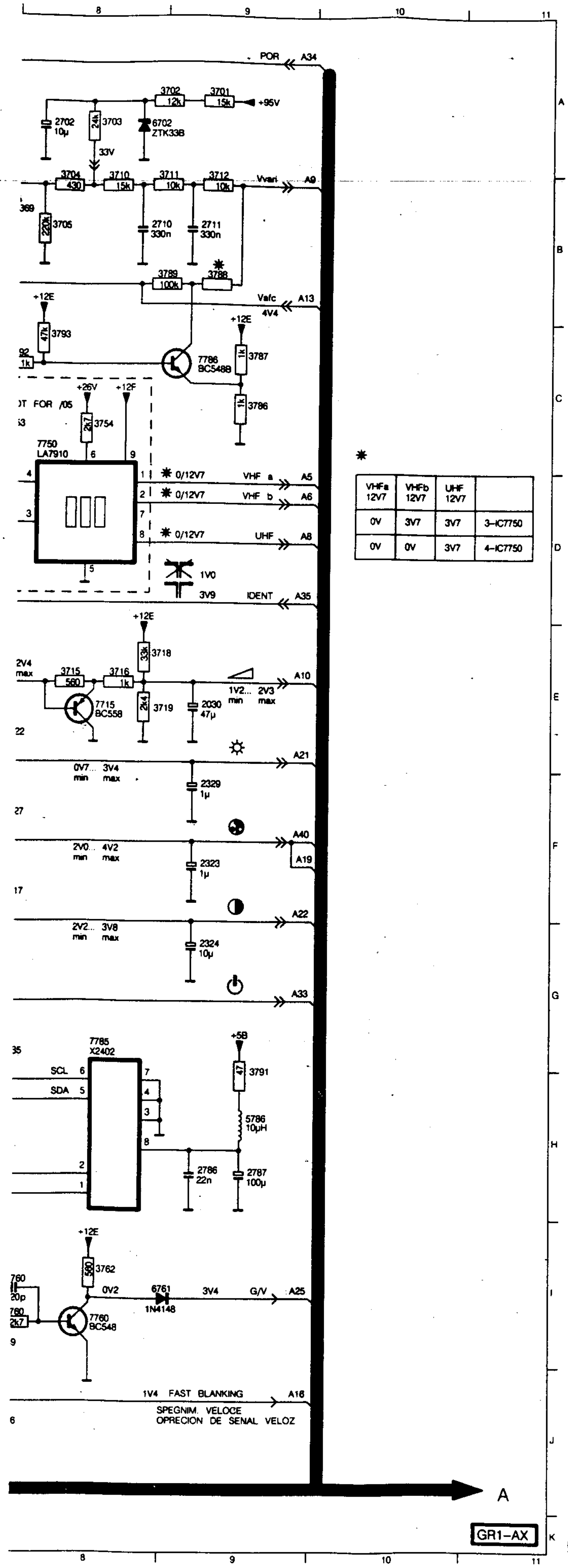
DIAGRAM-SCHALTBILD-SCHEMA-DIAGRAM A

(SUBJECT TO MODIFICATION)
(SOGGETTO A MODIFICHE)





CHROMINANCE + LUMINANCE
FARBART + LEUCHTDICHTE
CROMINANZA + LUMINANZA
CHROMINANCIA + LUMINANCIA
7300
TDA3565
A14 CHROMA/CROMA
CVBS
A15 LUM
IF SOUND/FI SUONO/SONIDO FI
Vafc
B16 FAST BLANKING/SPEGNIM. VELOCE
OPRECION DE SENAL VELOZ
1303
DL701
64μS
BURST
8.86MHz
DIV :2
F/F H/2
H/2
7040
BC548
7103
TDA7052
1020
SECAM/PAL
TRANSCODER
TRANSCODIFICATORE
TRANSCODIFICADOR
1326
500ns
BEAM INFO
INFORM. RAYO
INFORM. RAGGIO
SYNCHRONISATION-SINCRONIZZAZIONE-SYNCRONISMO
HORIZONTAL
ORIZZONTALE
7020-B
TDA8305
GATE
TOR SOGLIA
CIRCUITO DE PUERTA
PHASE 1
FASE 1
15625Hz
PHASE 2
FASE 2
FROM 7020-C (POINT 11)
INDENTIFICATION
INDENTIFICAZIONE
INDENTIFICACION
TO 7020-A (AFC)
BURST KEY
BURSTAUSTAST
ESTRAZIONE BURST
EXTRACCION BURST
BLANKING
RUCKLAUF-AUSTASTUNG
SPEGNIMENTO
OPRECION DE SENAL
50Hz
7046
BC558
7521
BC337
7523
BC337
VERTICAL
VERTIKAL
VERTICALE
7500
TDA3653B
BLANKING
RUCKLAUFAUSTAST
SPEGNIMENTO
VERTICAL FEEDBACK/REAZIONE VERT/REACCION VERT
B36 VERTICAL FLYBACK/RITORNO VERT/RETROCESO VERT



*

VHFa 12V7	VHFb 12V7	UHF 12V7	
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0V	0V	3V7	4-IC7750

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1785-D1
2030-E9
2323-F9
2324-G9
2329-F9
2702-A8
2710-B8
2711-B9
2715-E7
2735-E4
2736-E4
2737-F4
2738-F4
2760-I7
2769-I3
2771-J6
2777-I7
2778-I7
2779-C3
2780-C3
2782-B3
2785-D3
2786-H9
2787-H9
2790-B4
2791-B4
3326-J7
3701-A9
3702-A8
3703-A8
3704-B8
3705-B8
3706-B7
3707-B7
3710-B8
3711-B8
3712-B9
3715-E8
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3718-E8
3719-E8
3720-E7
3721-F7
3722-E7
3723-G7
3724-G7
3725-F7
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3737-F3
3738-F3
3739-G1
3740-F3
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3753-C7
3754-C8
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3757-C3
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3760-I7
3761-J7
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3765-H3
3767-H3
3768-I2
3769-I3
3770-I3
3771-J7
3773-J6
3780-D4
3781-B3
3784-H7
3785-H7
3786-C9
3787-C9
3788-B9
3789-B8
3791-H9
3792-C7
3793-C8
5752-D7
5753-D7
5777-I7
5785-H7
5786-H9
6300-J7
6702-A8
6715-E7
6735-G1
6736-G1
6737-G2
6757-C3
6761-I9
7700-H6
7705-B7
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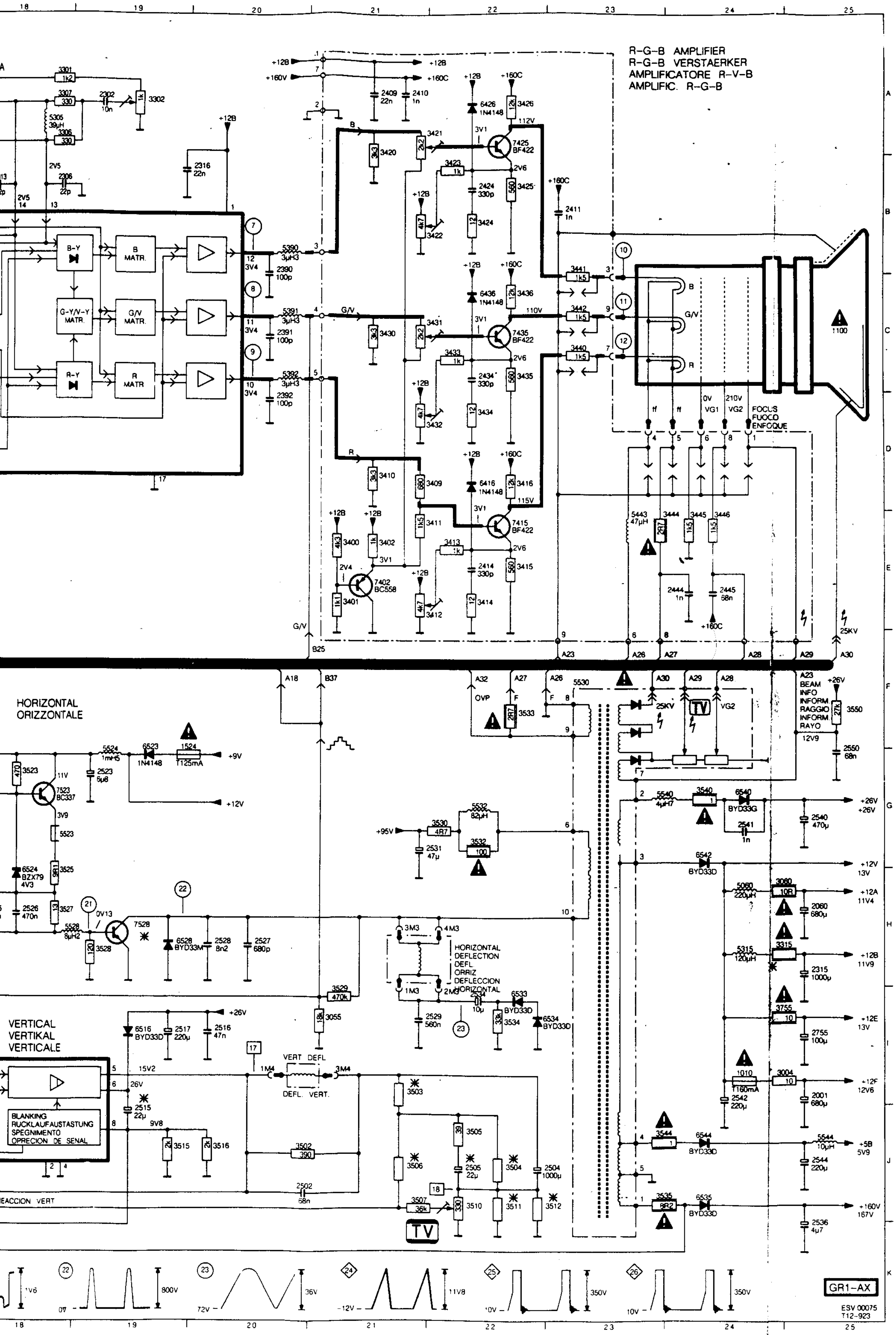
7786-C8

ESV 00085
T12-923



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1037-E5	3320-A13	6603-G4
1038-A11	3322-D16	6604-G4
1303-A17	3323-E16	6605-H4
1308-E17	3324-B12	6610-I 4
1326-B13	3327-B13	6613-F5
1524-G19	3328-B14	6614-J4
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1M6 -D13	3401-E21	6618-I 2
1M7 -E13	3402-E21	6620-I 5
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2001-J25	3410-D21	6635-J8
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2003-B2	3412-E21	6639-G9
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2005-B3	3414-E22	6641-G8
2021-D7	3415-E22	6642-G8
2023-J15	3416-D22	6643-G8
2025-C6	3420-B21	6644-G8
2026-J16	3421-A21	6645-G10
2027-C5	3422-B21	6646-G9
2029-F13	3423-B22	6647-G10
2031-D8	3424-B22	6671-I 8
2032-E9	3425-B22	6675-I 8
2033-E7	3426-A22	7020-A6
2034-F8	3430-C21	7020-J12
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2036-D6	3432-D21	7040-A10
2037-D5	3433-C22	7046-I 11
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2053-G11	3446-E24	7523-G18
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2306-B18	3514-I 16	CRT -B23
2308-E17	3515-J19	CRT -C21
2310-B16	3516-J20	CRT -D23
2311-B16	3520-G16	CRT -F24
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2316-B19	3525-H18	M3 -H21
2317-E14	3527-H18	M3 -I 22
2318-E15	3528-H19	M4 -I 20
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2328-B14	3533-F22	SPR3-C23
2342-E16	3534-I 22	SPR4-D24
2390-C20	3535-J23	SPR5-D23
2391-C20	3540-G24	SPR6-D24
2392-D20	3544-J23	SPR7-C23
2409-A21	3550-F25	SPR8-D24
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2444-E24	3612-I 4	
2445-E24	3613-H4	
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2502-J20	3615-I 3	
2504-J22	3616-H5	
2505-J22	3617-I 2	
2514-J17	3618-I 2	
2515-J19	3619-I 2	
2516-I 20	3625-F7	
2517-I 19	3626-G7	
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2528-H20	3635-J7	
2529-I 21	3642-H9	
2531-H21	3668-H7	
2534-I 22	3669-H8	
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2541-G24	3680-I 5	
2542-J24	3755-I 24	
2544-J25	3M6 -D13	
2550-G25	3M7 -E13	
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2606-H4	5035-E6	
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2M7 -E13	5524-G19	
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3025-I 16	5600-F3	
3027-C5	5601-G2	
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3045-H17	5617-I 2	
3046-H11	5620-I 5	
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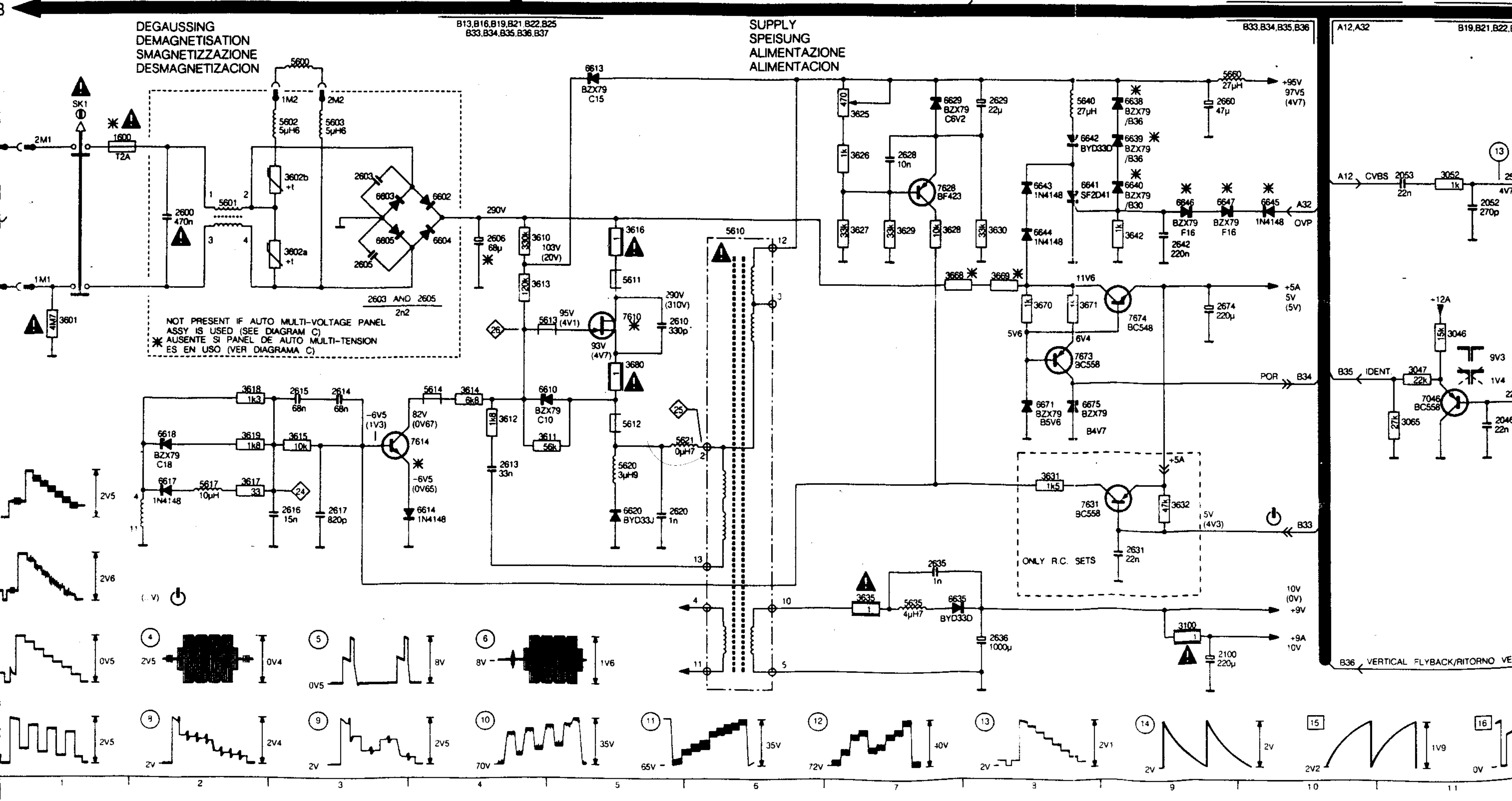
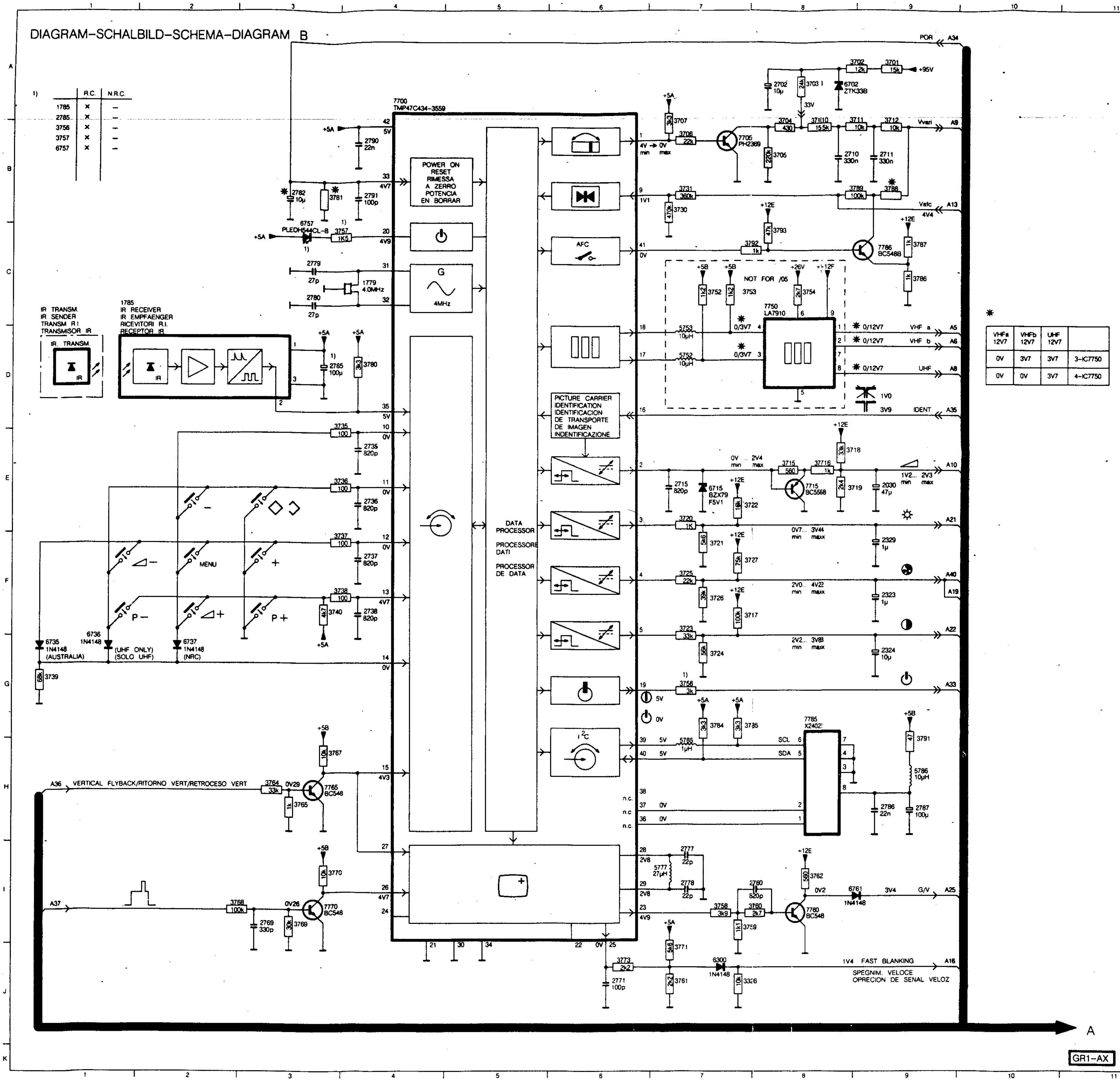


DEGAUSSING
DEMAGNETISATION
SMAGNETIZZAZIONE
DESMAGNETIZACION
SUPPLY
SPEISUNG
ALIMENTAZIONE
ALIMENTACION
B13,B16,B19,B21,B22,B25
B33,B34,B35,B36,B37
B33,B34,B35,B36
A12,A32
NOT PRESENT IF AUTO MULTI-VOLTAGE PANEL ASSY IS USED (SEE DIAGRAM C)
AUSENTE SI PANEL DE AUTO MULTI-TENSION ES EN USO (VER DIAGRAMA C)
2603 AND 2605
2n2
ONLY R.C. SETS
+95V
97V5
(4V7)
+5A
5V
(5V)
POR
IDENT.
CVBS
OVP
10V
(0V)
+9V
+9A
10V
VERTICAL FLYBACK/RITORNO VE



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2030-E9
2323-F9
2324-G9
2329-F9
2702-A8
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2715-E7
2735-E4
2736-E4
2737-F4
2738-F4
2760-I7
2769-I3
2771-J6
2777-I7
2778-I7
2779-C3
2780-C3
2782-B3
2785-D3
2786-H9
2787-H9
2790-B4
2791-B4
3326-J7
3701-A9
3702-A8
3703-A8
3704-B8
3705-B8
3706-B7
3707-B7
3710-B8
3711-B8
3712-B9
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3716-E8
3717-F7
3718-E8
3719-E8
3720-E7
3721-F7
3722-E7
3723-G7
3724-G7
3725-F7
3726-F7
3727-F7
3730-C7
3731-B7
3735-E3
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3737-F3
3738-F3
3739-G1
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3759-J7
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3761-J7
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3764-H3
3765-H3
3767-H3
3768-I2
3769-I3
3770-I3
3771-J7
3773-J6
3780-D4
3781-B3
3784-H7
3785-H7
3786-C9
3787-C9
3788-B9
3789-B8
3791-H9
3792-C7
3793-C8
5752-D7
5753-D7
5777-I7
5785-H7
5786-H9
6300-J7
6702-A8
6715-E7
6735-G1
6736-G1
6737-G2
6757-C3
6761-I9
7700-H6
7705-B7
7715-E8
7750-D8
7760-I8
7765-H3
7770-I3
7786-C8

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